



Q77H2-AS B75H2-AS

Rev : 1.0


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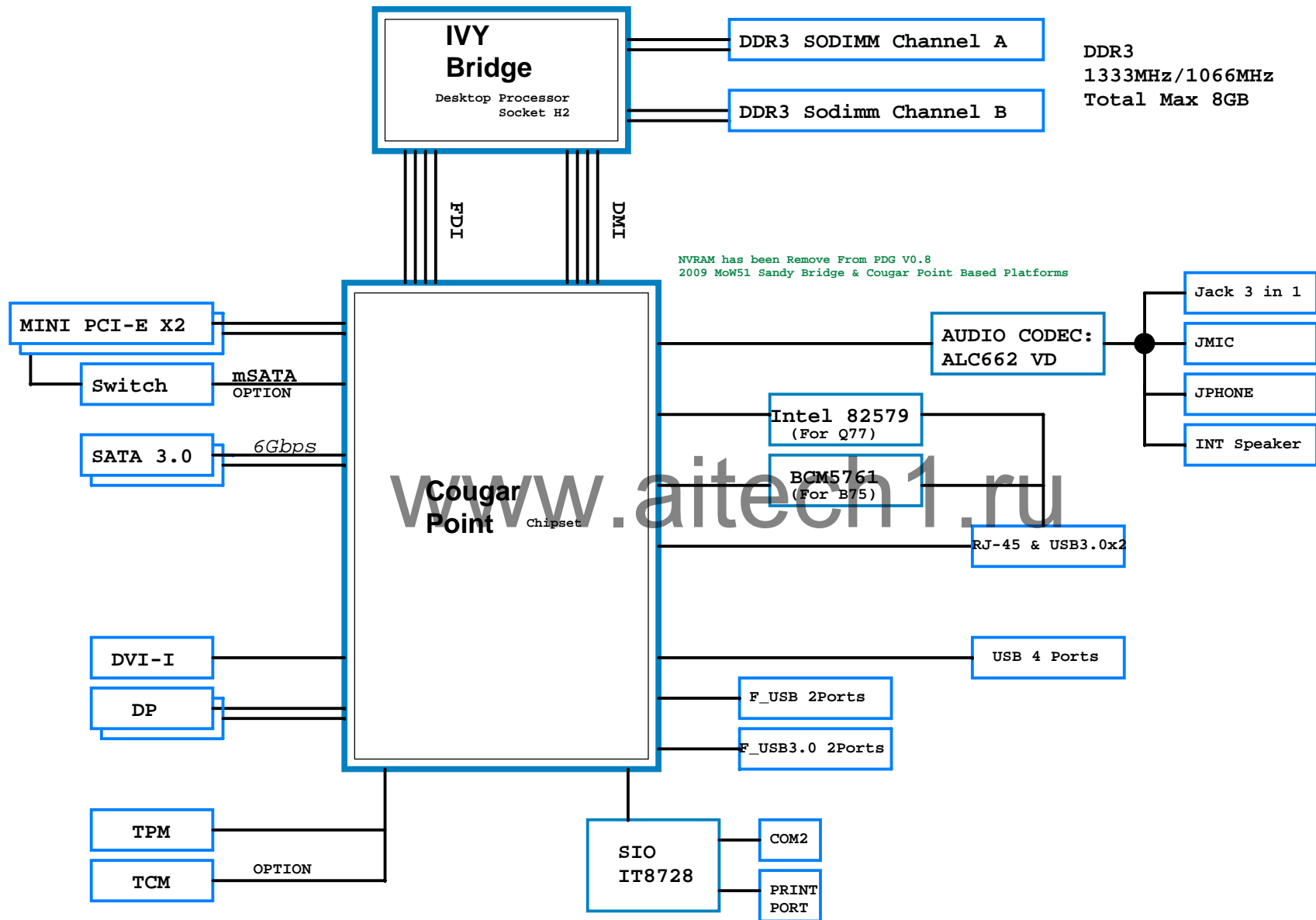
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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/09/05	Initial version
V.B	2011/12/22	
V.1.0	2012/02/03	

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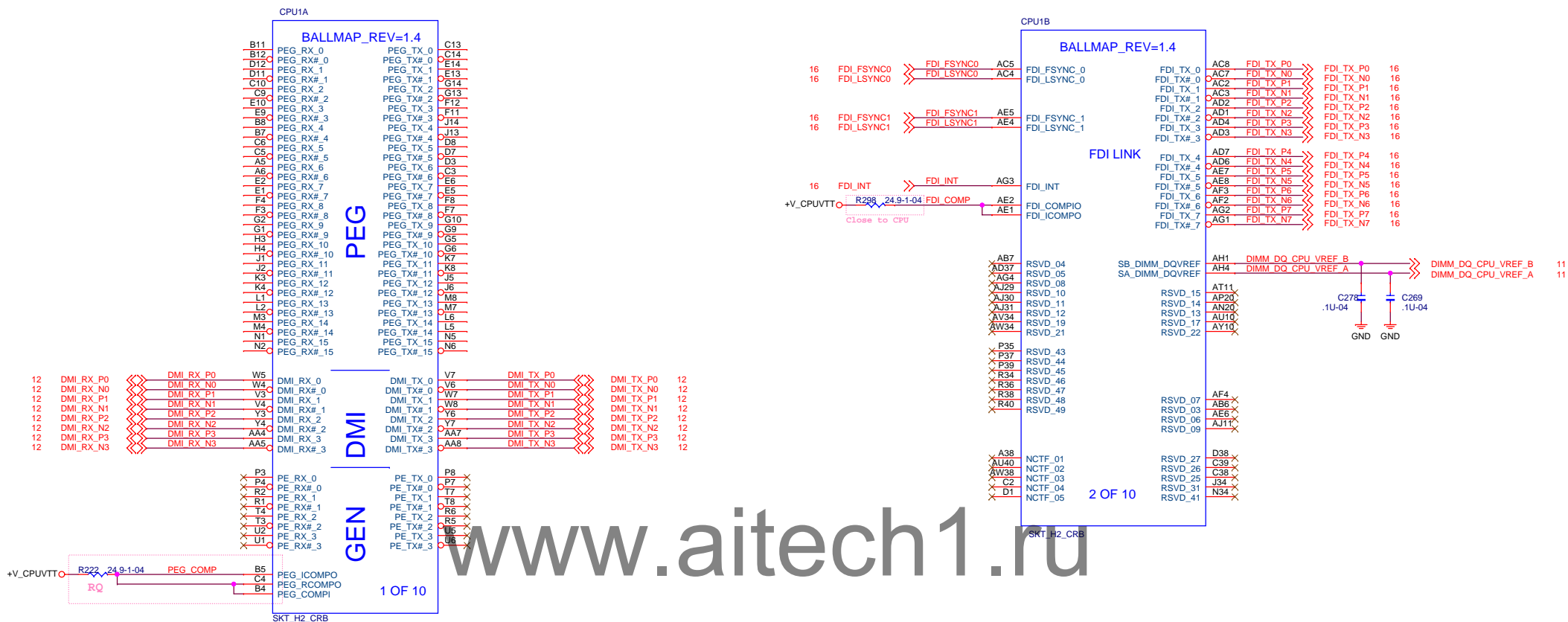
PCH-GPIO function

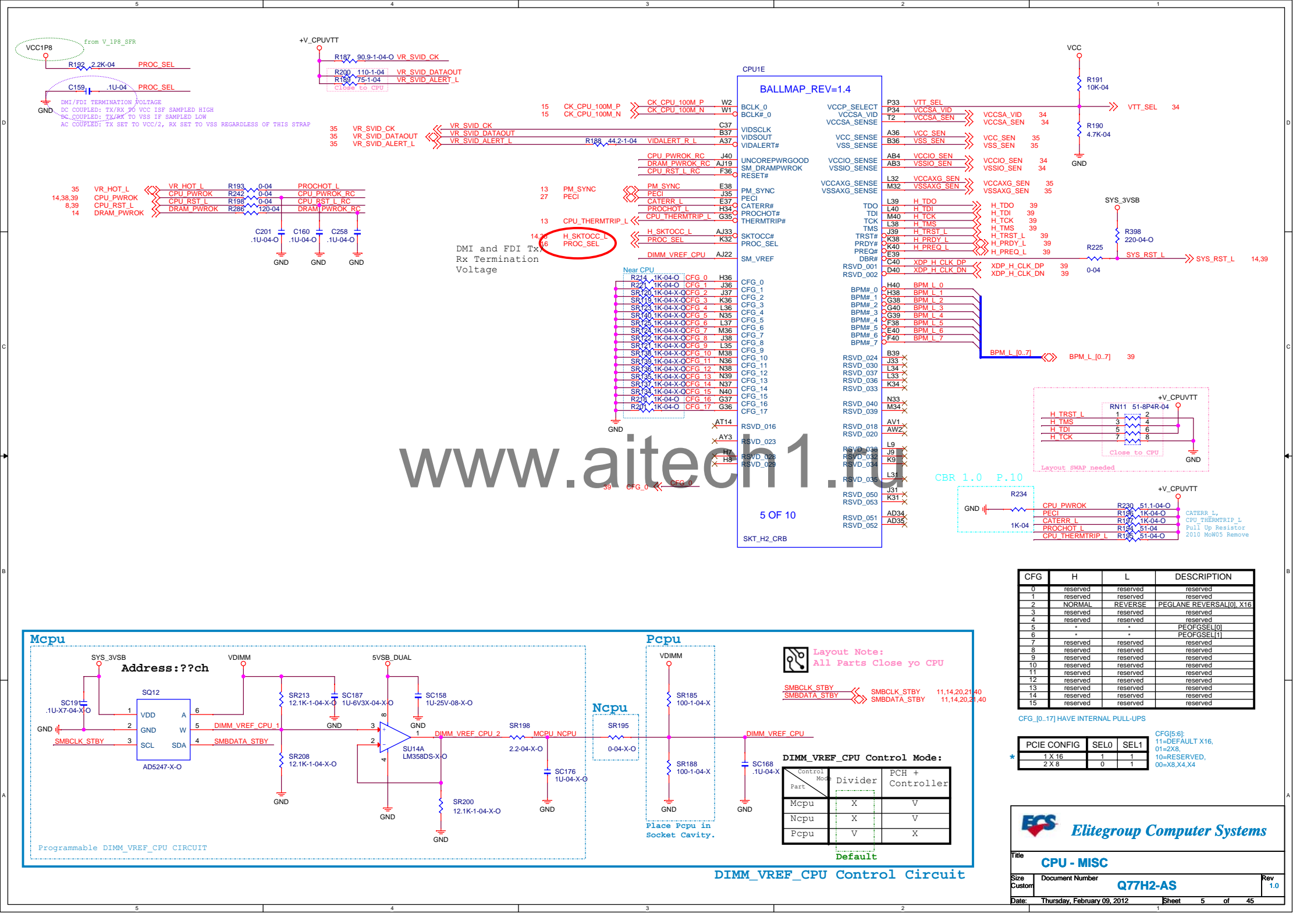
Pin Name	Power Well	Function	Default Status
GPIO0	VCC3	Case Open(Reserve)	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal shutdown	GPI
GPIO13	3VSB	LPC_PME_L	GPI
GPIO15	3VSB	TLS_EN	GPO
GPIO20	VCC3	SPI_WP_L	Native
GPIO27	DSW	PCH_GP27	GPI
GPIO28	3VSB	ON_DIE_PLL_EN	GPO
GPIO45	3VSB	SPI_WPSW	Native
GPIO57	3VSB	SPI_WP0_L	GPI
GPIO61	3VSB	LPCPD_L	Native
GPIO72	3VSB	GPIO72_S4S5	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		SIO_BEEP	
GP22		Power LED	
GP64		MB_ID0	
GP63		MB_ID1	
GP17		MB_ID2	
GP14		Thermal shutdown	
GP47		BS3 (Acer Reserve)	
GP66		BS2 (Acer Reserve)	

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9	M_DATA_A[0..63]	←	M_DATA A[0..63]
9	M_DQS_A_P[0..7]	←	M DQS A P[0..7]
9	M_DQS_A_N[0..7]	←	M DQS A N[0..7]
9	M_MA_A[0..15]	←	M MA A[0..15]
9	M_BS_A[0..2]	←	M BS A[0..2]
9	M_CS_A_L[0..1]	←	M CS A L[0..1]
9	M_CKE_A[0..1]	←	M CKE A[0..1]
9	M_ODT_A[0..1]	←	M ODT A[0..1]
9	M_CLK_A_P[0..1]	←	M CLK A P[0..1]
9	M_CLK_A_N[0..1]	←	M CLK A N[0..1]
9	M_WE_A_L	←	M WE A L
9	M_CAS_A_L	←	M CAS A L
9	M_RAS_A_L	←	M RAS A L

DDR3 CH.A

9 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

9	M_DATA_B[0..63]	←	M_DATA B[0..63]
9	M_DQS_B_P[0..7]	←	M DQS B P[0..7]
9	M_DQS_B_N[0..7]	←	M DQS B N[0..7]
9	M_MA_B[0..15]	←	M MA B[0..15]
9	M_BS_B[0..2]	←	M BS B[0..2]
9	M_CS_B_L[0..1]	←	M CS B L[0..1]
9	M_CKE_B[0..1]	←	M CKE B[0..1]
9	M_ODT_B[0..1]	←	M ODT B[0..1]
9	M_CLK_B_P[0..1]	←	M CLK B P[0..1]
9	M_CLK_B_N[0..1]	←	M CLK B N[0..1]
9	M_WE_B_L	←	M WE B L
9	M_CAS_B_L	←	M CAS B L
9	M_RAS_B_L	←	M RAS B L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AL1	SA_DQ_7
M_DATA_A8	AN1	SA_MA_8
M_DATA_A9	AN4	SA_DQ_8
M_DATA_A10	AR3	SA_DQ_9
M_DATA_A11	AR4	SA_DQ_10
M_DATA_A12	AN2	SA_DQ_11
M_DATA_A13	AN3	SA_DQ_12
M_DATA_A14	AR2	SA_DQ_13
M_DATA_A15	AR1	SA_DQ_14
M_DATA_A16	AV2	SA_DQ_15
M_DATA_A17	AV3	SA_DQ_16
M_DATA_A18	AV5	SA_DQ_17
M_DATA_A19	AW5	SA_DQ_18
M_DATA_A20	AU2	SA_DQ_19
M_DATA_A21	AU3	SA_DQ_20
M_DATA_A22	AU5	SA_DQ_21
M_DATA_A23	AV7	SA_DQ_22
M_DATA_A24	AY7	SA_DQ_23
M_DATA_A25	AU7	SA_DQ_24
M_DATA_A26	AV9	SA_DQ_25
M_DATA_A27	AU9	SA_DQ_26
M_DATA_A28	AV7	SA_DQ_27
M_DATA_A29	AV7	SA_DQ_28
M_DATA_A30	AW9	SA_DQ_29
M_DATA_A31	AY9	SA_DQ_30
M_DATA_A32	AU35	SA_DQ_31
M_DATA_A33	AW37	SA_DQ_32
M_DATA_A34	AU39	SA_DQ_33
M_DATA_A35	AU36	SA_DQ_34
M_DATA_A36	AW35	SA_DQ_35
M_DATA_A37	AY36	SA_DQ_36
M_DATA_A38	AU38	SA_DQ_37
M_DATA_A39	AU37	SA_DQ_38
M_DATA_A40	AR40	SA_DQ_39
M_DATA_A41	AR37	SA_DQ_40
M_DATA_A42	AN38	SA_DQ_41
M_DATA_A43	AN37	SA_DQ_42
M_DATA_A44	AR39	SA_DQ_43
M_DATA_A45	AR38	SA_DQ_44
M_DATA_A46	AN39	SA_DQ_45
M_DATA_A47	AN40	SA_DQ_46
M_DATA_A48	AL40	SA_DQ_47
M_DATA_A49	AL37	SA_DQ_48
M_DATA_A50	AJ38	SA_DQ_49
M_DATA_A51	AJ37	SA_DQ_50
M_DATA_A52	AE38	SA_DQ_51
M_DATA_A53	AL38	SA_DQ_52
M_DATA_A54	AJ39	SA_DQ_53
M_DATA_A55	AJ40	SA_DQ_54
M_DATA_A56	AG40	SA_DQ_55
M_DATA_A57	AG37	SA_DQ_56
M_DATA_A58	AE38	SA_DQ_57
M_DATA_A59	AE37	SA_DQ_58
M_DATA_A60	AG39	SA_DQ_59
M_DATA_A61	AG38	SA_DQ_60
M_DATA_A62	AE39	SA_DQ_61
M_DATA_A63	AE40	SA_DQ_62
M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AV4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AV8	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SA_MA_0	AV27	M MA A0
SA_MA_1	AV24	M MA A1
SA_MA_2	AW24	M MA A2
SA_MA_3	AW23	M MA A3
SA_MA_4	AV23	M MA A4
SA_MA_5	AT24	M MA A5
SA_MA_6	AV22	M MA A6
SA_MA_7	AV22	M MA A7
SA_MA_8	AT22	M MA A8
SA_MA_9	AT21	M MA A9
SA_MA_10	AV28	M MA A10
SA_MA_11	AT21	M MA A11
SA_MA_12	AW32	M MA A12
SA_MA_13	AU20	M MA A13
SA_MA_14	AU20	M MA A14
SA_MA_15	AT20	M MA A15
SA_WE#	AW29	M WE A L
SA_CAS#	AV30	M CAS A L
SA_RAS#	AU28	M RAS A L
SA_BS_0	AV29	M BS A0
SA_BS_1	AW28	M BS A1
SA_BS_2	AV20	M BS A2
SA_CS#_0	AV29	M CS A L0
SA_CS#_1	AU30	M CS A L1
SA_CS#_2	AW30	M CS A L1
SA_CS#_3	AU33	M CS A L1
SA_CKE_0	AV19	M CKE A0
SA_CKE_1	AT19	M CKE A1
SA_CKE_2	AV18	M CKE A1
SA_CKE_3	AV18	M CKE A1
SA_ODT_0	AV31	M ODT A0
SA_ODT_1	AU32	M ODT A1
SA_ODT_2	AU30	M ODT A1
SA_ODT_3	AW33	M ODT A1
SA_CK_0	AY25	M CLK A P0
SA_CK#_0	AW25	M CLK A N0
SA_CK_1	AU24	M CLK A P1
SA_CK#_1	AW25	M CLK A N1
SA_CK_2	AV27	M CLK A P1
SA_CK#_2	AV26	M CLK A N1
SA_CK_3	AW26	M CLK A N1

SM_DRAMRST# AW18DDR3_DRAMRST_R L R514 0-04 DDR3_DRAMRST_L

SA_DQS_8 SA_DQS#_8

SA_ECC_CB_0 SA_ECC_CB_1 SA_ECC_CB_2 SA_ECC_CB_3 SA_ECC_CB_4 SA_ECC_CB_5 SA_ECC_CB_6 SA_ECC_CB_7

DDR_0
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SKT_H2_CRB

DDR3 CH.A

Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AP7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AP9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR32	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B52	AM31	SB_DQ_49
M_DATA_B55	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B57	AH35	SB_DQ_56
M_DATA_B58	AE34	SB_DQ_57
M_DATA_B59	AE35	SB_DQ_58
M_DATA_B60	AJ35	SB_DQ_59
M_DATA_B61	AJ34	SB_DQ_60
M_DATA_B62	AF33	SB_DQ_61
M_DATA_B63	AF35	SB_DQ_62
M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7
M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN26	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

SA_DQS_8 SB_DQS#_8

SB_ECC_CB_0 SB_ECC_CB_1 SB_ECC_CB_2 SB_ECC_CB_3 SB_ECC_CB_4 SB_ECC_CB_5 SB_ECC_CB_6 SB_ECC_CB_7

DDR_1
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SKT_H2_CRB

DDR3 CH.B

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AP7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AP9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR32	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B52	AM31	SB_DQ_49
M_DATA_B55	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B57	AH35	SB_DQ_56
M_DATA_B58	AE34	SB_DQ_57
M_DATA_B59	AE35	SB_DQ_58
M_DATA_B60	AJ35	SB_DQ_59
M_DATA_B61	AJ34	SB_DQ_60
M_DATA_B62	AF33	SB_DQ_61
M_DATA_B63	AF35	SB_DQ_62
M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7
M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN26	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

SA_DQS_8 SB_DQS#_8

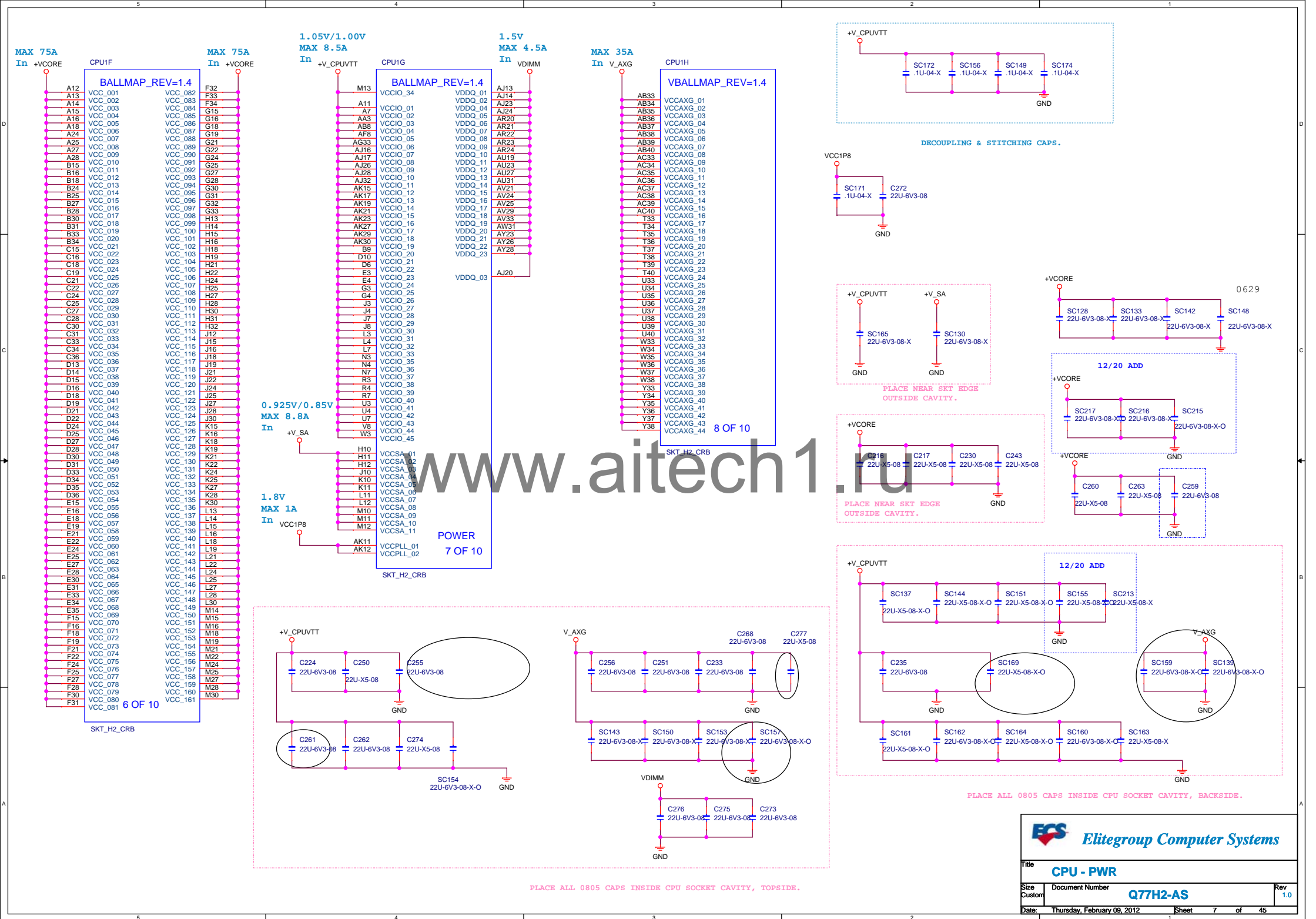
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Desktop doesn't support ECC

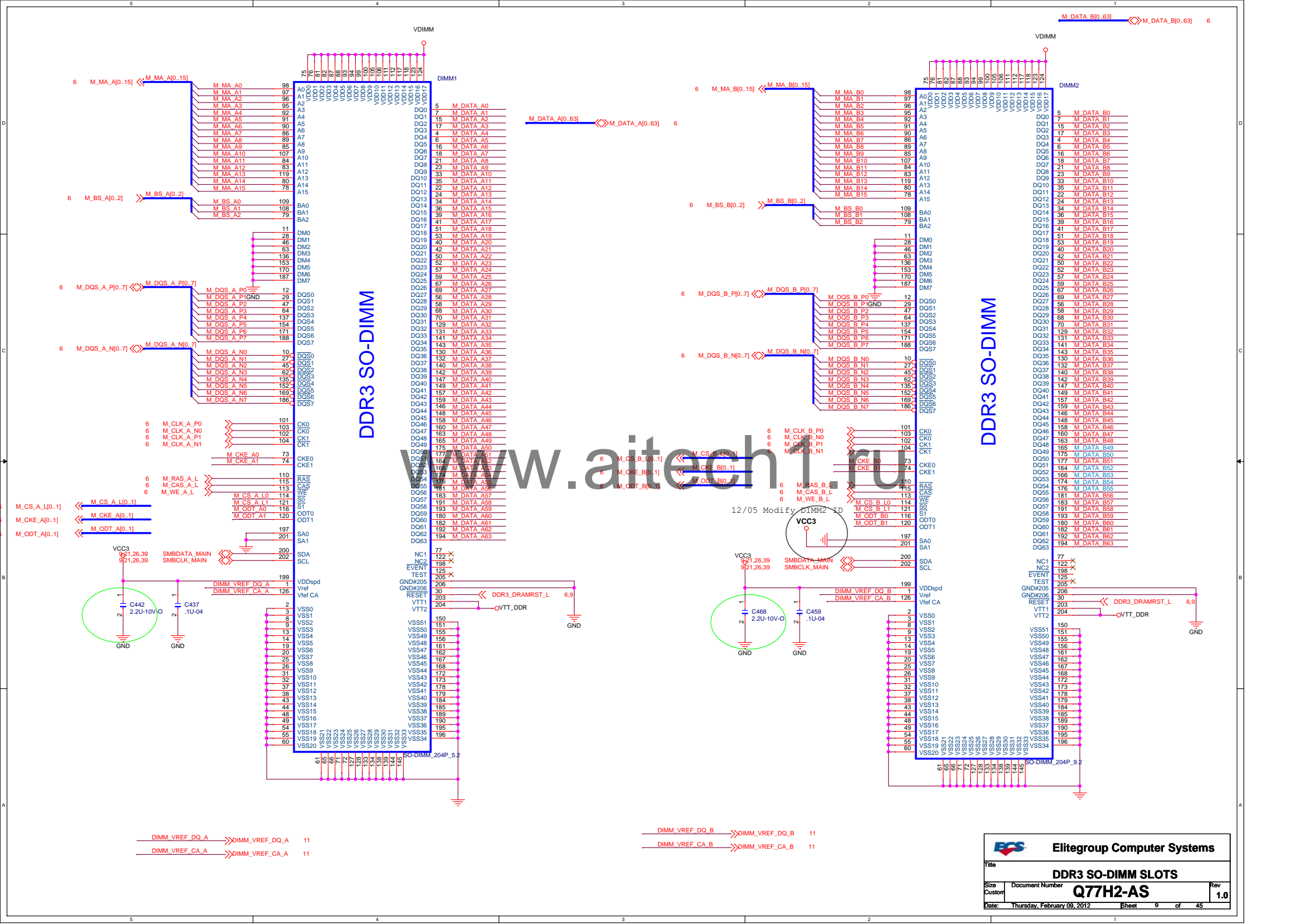


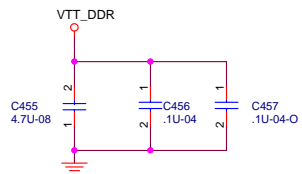
Elitegroup Computer Systems

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CPU - DDR3			
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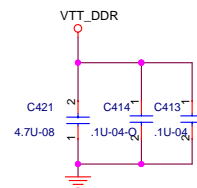
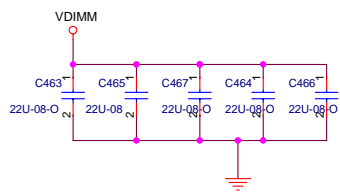
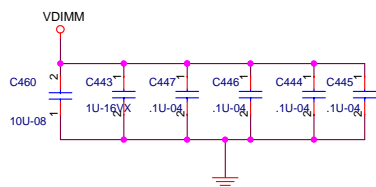


CPU1I				CPU1J			
BALLMAP_REV=1.4				BALLMAP_REV=1.4			
A17	VSS_001	VSS_091	AM27	AV11	VSS_181	VSS_271	G8
A23	VSS_002	VSS_092	AM3	AV14	VSS_182	VSS_272	H1
A26	VSS_003	VSS_093	AM30	AV17	VSS_183	VSS_273	H17
A29	VSS_004	VSS_094	AM36	AV3	VSS_184	VSS_274	H2
AA35	VSS_005	VSS_095	AM37	AV35	VSS_185	VSS_275	H20
AA33	VSS_006	VSS_096	AM38	AV38	VSS_186	VSS_276	H23
AA34	VSS_007	VSS_097	AM39	AV6	VSS_187	VSS_277	H26
AA35	VSS_008	VSS_098	AM4	AW10	VSS_188	VSS_278	H29
AA36	VSS_009	VSS_099	AM40	AW11	VSS_189	VSS_279	H33
AA37	VSS_010	VSS_100	AM5	AW14	VSS_190	VSS_280	H35
AA38	VSS_011	VSS_101	AN10	AW16	VSS_191	VSS_281	H37
AA6	VSS_012	VSS_102	AN11	AW36	VSS_192	VSS_282	H39
AB5	VSS_013	VSS_103	AN12	AW6	VSS_193	VSS_283	H5
AC1	VSS_014	VSS_104	AN14	AY11	VSS_194	VSS_284	H6
AC6	VSS_015	VSS_105	AN17	AY14	VSS_195	VSS_285	H9
AD33	VSS_016	VSS_106	AN22	AY18	VSS_196	VSS_286	J11
AD36	VSS_017	VSS_107	AN24	AY35	VSS_197	VSS_287	J17
AD38	VSS_018	VSS_108	AN30	AY6	VSS_198	VSS_288	J20
AD39	VSS_019	VSS_109	AN31	AY8	VSS_199	VSS_289	J23
AD40	VSS_020	VSS_110	AN31	AY8	VSS_200	VSS_290	J26
AD5	VSS_021	VSS_111	AN32	B10	VSS_201	VSS_291	J29
AD8	VSS_022	VSS_112	AN33	B13	VSS_202	VSS_292	J32
AE3	VSS_023	VSS_113	AN34	B14	VSS_203	VSS_293	K1
AE33	VSS_024	VSS_114	AN35	B17	VSS_204	VSS_294	K12
AE36	VSS_025	VSS_115	AN36	B23	VSS_205	VSS_295	K13
AF1	VSS_026	VSS_116	AN5	B26	VSS_206	VSS_296	K14
AF34	VSS_027	VSS_117	AN7	B32	VSS_207	VSS_297	K17
AF36	VSS_028	VSS_118	AN8	B35	VSS_208	VSS_298	K20
AF40	VSS_029	VSS_119	AN9	B38	VSS_209	VSS_299	K23
AF5	VSS_030	VSS_120	AP1	B6	VSS_210	VSS_300	K26
AF6	VSS_031	VSS_121	AP11	B11	VSS_211	VSS_301	K29
AF7	VSS_032	VSS_122	AP17	C11	VSS_212	VSS_302	K33
AG36	VSS_033	VSS_123	AP14	C12	VSS_213	VSS_303	K35
AH2	VSS_034	VSS_124	AP22	C20	VSS_214	VSS_304	K37
AH3	VSS_035	VSS_125	AP25	C23	VSS_215	VSS_305	K39
AH33	VSS_036	VSS_126	AP26	C26	VSS_216	VSS_306	K5
AH36	VSS_037	VSS_127	AP27	C29	VSS_217	VSS_307	K6
AH37	VSS_038	VSS_128	AP30	C36	VSS_218	VSS_308	K10
AH38	VSS_039	VSS_129	AP37	C37	VSS_219	VSS_309	K17
AH39	VSS_040	VSS_130	AP4	C7	VSS_220	VSS_310	L20
AH40	VSS_041	VSS_131	AP5	D8	VSS_221	VSS_311	L23
AH5	VSS_042	VSS_132	AP40	D17	VSS_222	VSS_312	L26
AH8	VSS_043	VSS_133	AP5	D2	VSS_223	VSS_313	L29
AH12	VSS_044	VSS_134	AR14	D20	VSS_224	VSS_314	L8
AJ15	VSS_045	VSS_135	AR17	D23	VSS_225	VSS_315	M1
AJ18	VSS_046	VSS_136	AR18	D26	VSS_226	VSS_316	M17
AJ21	VSS_047	VSS_137	AR19	D29	VSS_227	VSS_317	M2
AJ25	VSS_048	VSS_138	AR27	D32	VSS_228	VSS_318	M20
AJ27	VSS_049	VSS_139	AR30	D37	VSS_229	VSS_319	M23
AJ36	VSS_050	VSS_140	AR36	D39	VSS_230	VSS_320	M28
AJ5	VSS_051	VSS_141	AR5	D31	VSS_231	VSS_321	M29
AK1	VSS_052	VSS_142	AT1	D4	VSS_232	VSS_322	M33
AK10	VSS_053	VSS_143	AT10	D5	VSS_233	VSS_323	M35
AK14	VSS_054	VSS_144	AT12	D9	VSS_234	VSS_324	M37
AK17	VSS_055	VSS_145	AT13	E11	VSS_235	VSS_325	M39
AK16	VSS_056	VSS_146	AT15	E17	VSS_236	VSS_326	M5
AK22	VSS_057	VSS_147	AT16	E20	VSS_237	VSS_327	M6
AK28	VSS_058	VSS_148	AT17	E23	VSS_238	VSS_328	M9
AK29	VSS_059	VSS_149	AT12	E26	VSS_239	VSS_329	N8
AK31	VSS_060	VSS_150	AT27	E29	VSS_240	VSS_330	N9
AK32	VSS_061	VSS_151	AT27	E32	VSS_241	VSS_331	P1
AK33	VSS_062	VSS_152	AT28	E36	VSS_242	VSS_332	P2
AK34	VSS_063	VSS_153	AT29	E7	VSS_243	VSS_333	P36
AK35	VSS_064	VSS_154	AT3	E8	VSS_244	VSS_334	P38
AK36	VSS_065	VSS_155	AT3	F1	VSS_245	VSS_335	P40
AK37	VSS_066	VSS_156	AT30	F10	VSS_246	VSS_336	P5
AK4	VSS_067	VSS_157	AT31	F13	VSS_247	VSS_337	P6
AK5	VSS_068	VSS_158	AT33	F14	VSS_248	VSS_338	R33
AK6	VSS_069	VSS_159	AT34	F17	VSS_249	VSS_339	R35
AK7	VSS_070	VSS_160	AT35	F20	VSS_250	VSS_340	R37
AK8	VSS_071	VSS_161	AT36	F23	VSS_251	VSS_341	R39
AK9	VSS_072	VSS_162	AT37	F26	VSS_252	VSS_342	T1
AL11	VSS_073	VSS_163	AT38	F29	VSS_253	VSS_343	T5
AL14	VSS_074	VSS_164	AT39	F29	VSS_254	VSS_344	T6
AL17	VSS_075	VSS_165	AT4	F35	VSS_255	VSS_345	T8
AL19	VSS_076	VSS_166	AT40	F37	VSS_256	VSS_346	U1
AL24	VSS_077	VSS_167	AT5	F39	VSS_257	VSS_347	U8
AL27	VSS_078	VSS_168	AT6	F5	VSS_258	VSS_348	V2
AL30	VSS_079	VSS_169	AT7	F6	VSS_259	VSS_349	V33
AL36	VSS_080	VSS_170	AT8	F9	VSS_260	VSS_350	V34
AL5	VSS_081	VSS_171	AT9	G11	VSS_261	VSS_351	V35
AM1	VSS_082	VSS_172	AT15	G12	VSS_262	VSS_352	V36
AM11	VSS_083	VSS_173	AU1	G17	VSS_263	VSS_353	V37
AM14	VSS_084	VSS_174	AU26	G17	VSS_264	VSS_354	V38
AM17	VSS_085	VSS_175	AU34	G23	VSS_265	VSS_355	V39
AM2	VSS_086	VSS_176	AU4	G26	VSS_266	VSS_356	V40
AM21	VSS_087	VSS_177	AU6	G29	VSS_267	VSS_357	V5
AM23	VSS_088	VSS_178	AU8	G34	VSS_268	VSS_358	W6
AM25	VSS_089	VSS_179	AV10	G7	VSS_269	VSS_359	Y5
AM25	VSS_090	VSS_180			VSS_270	VSS_360	Y8
A4	VSS_NCTF_01			AY37	VSS_NCTF_03		
AV39	VSS_NCTF_02	9 OF 10		B3	VSS_NCTF_04	10 OF 10	
GND				GND			
SKT_H2_CRB				SKT_H2_CRB			

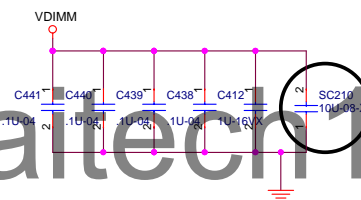




Layout: Close to DIMM0



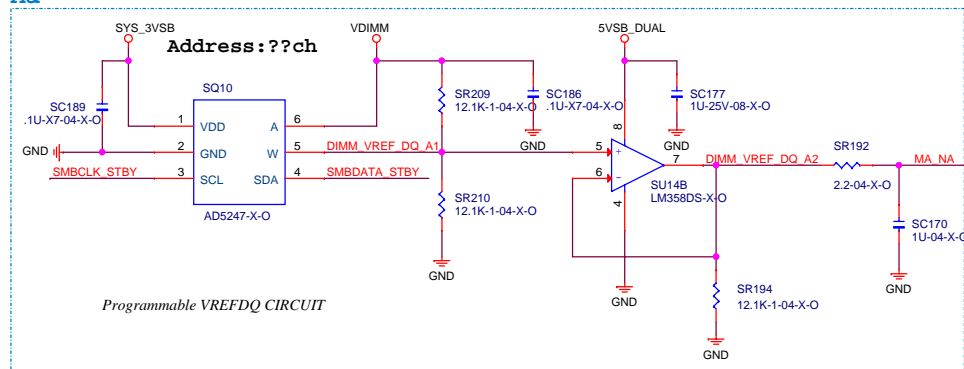
Layout: Close to DIMM1



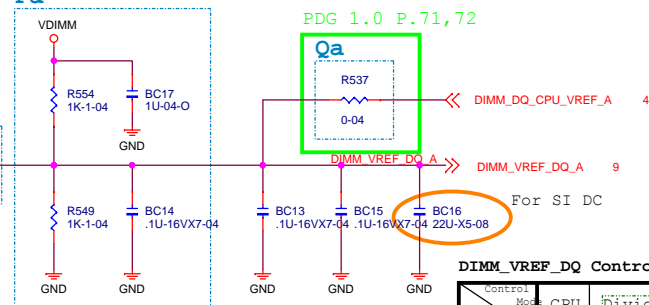
Elitegroup Computer Systems

Title			DDR3 SODIMM CAPACITOR	
Size			Document Number	
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Ma

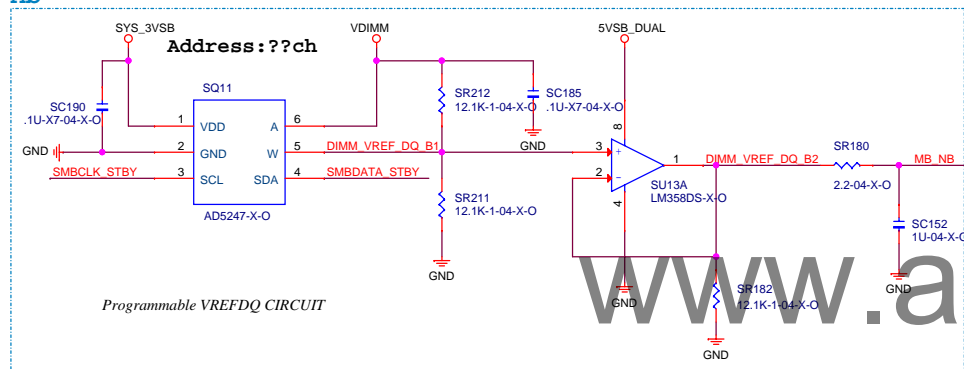


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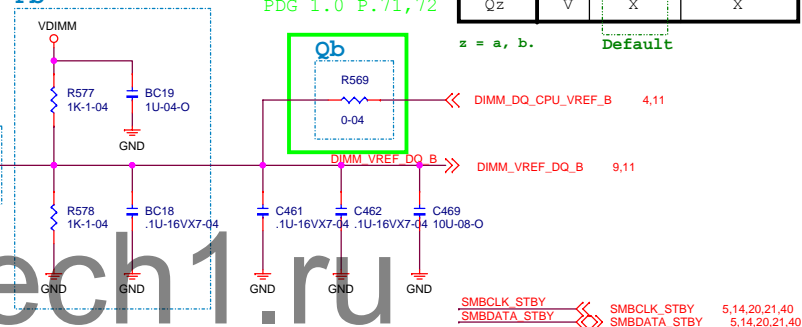


Layout Note:
All parts close to DDR3 Slots.

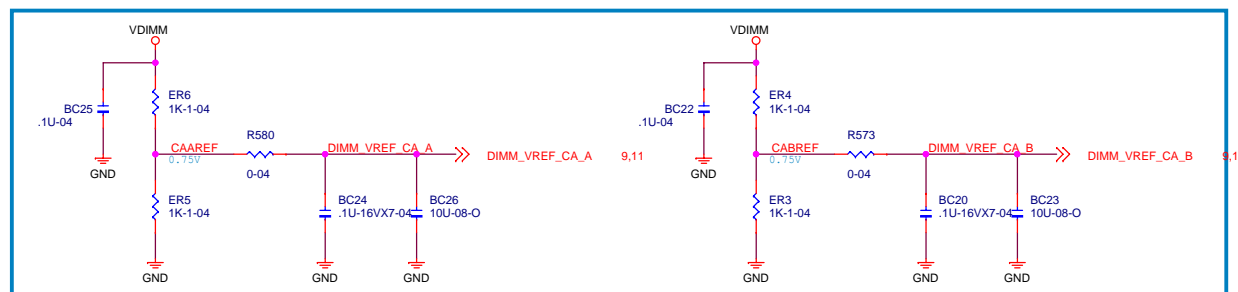
Mb



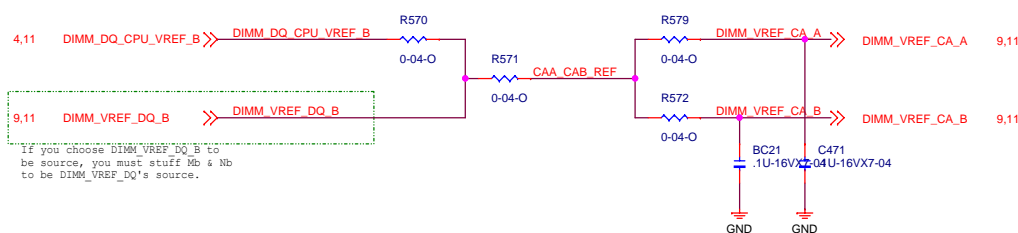
Pb



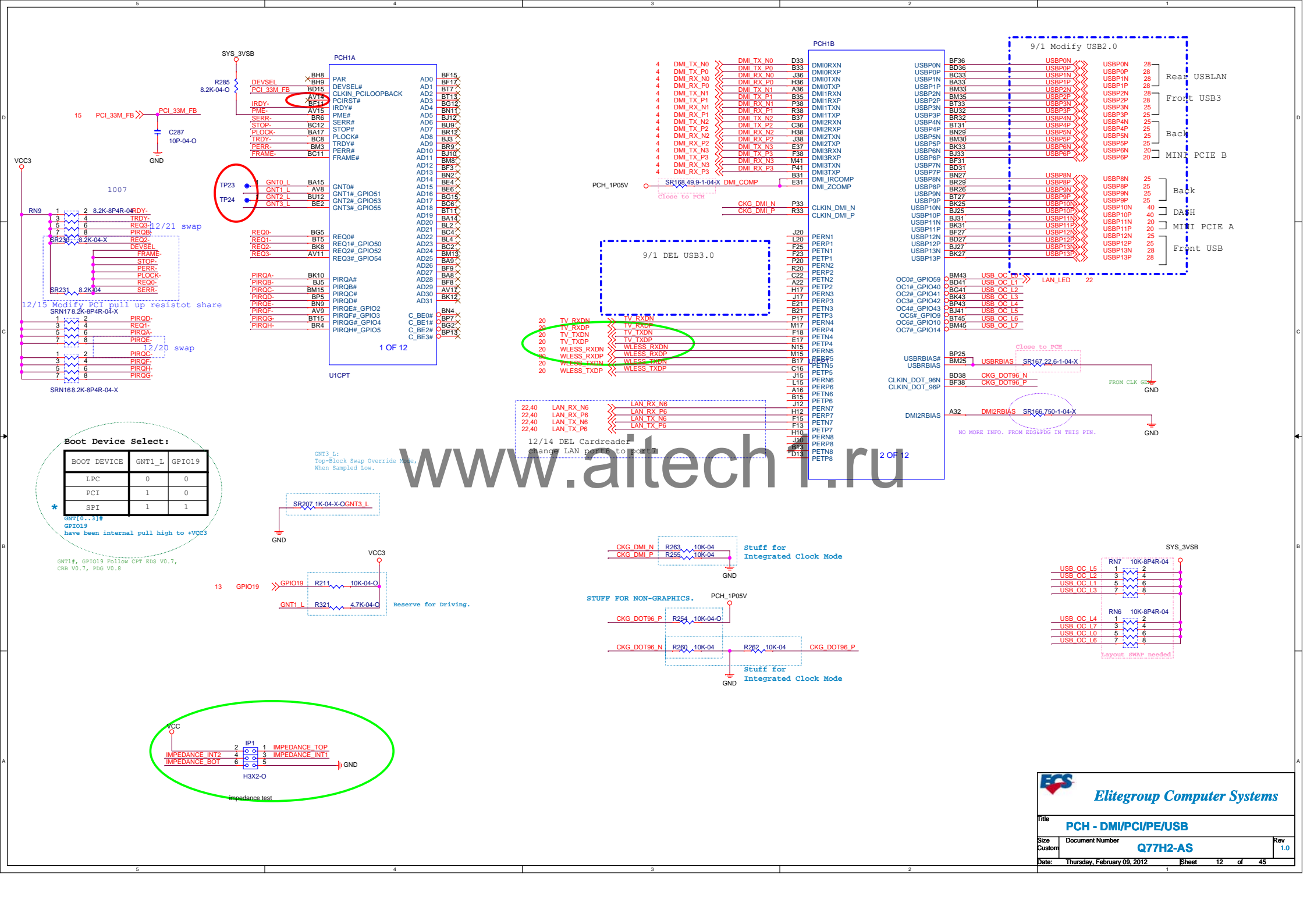
DIMM_VREF_DQ Control Circuit

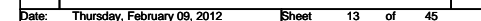


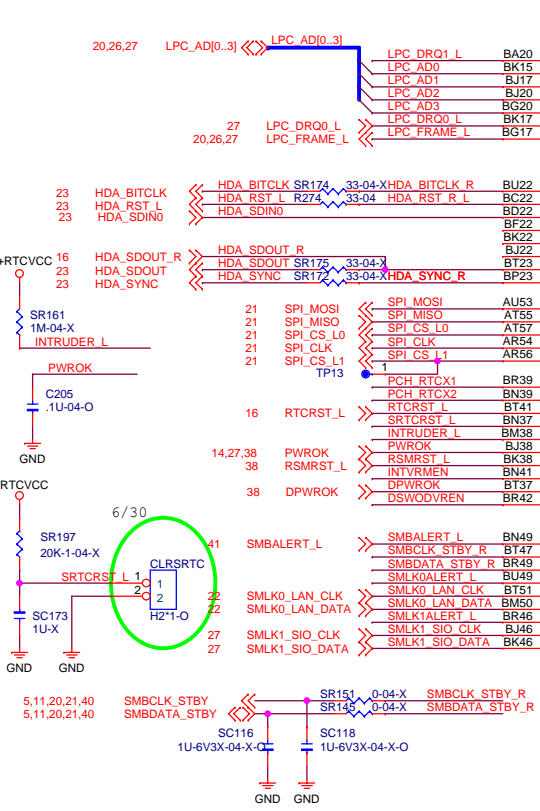
DIMM_VREF_CA Circuit



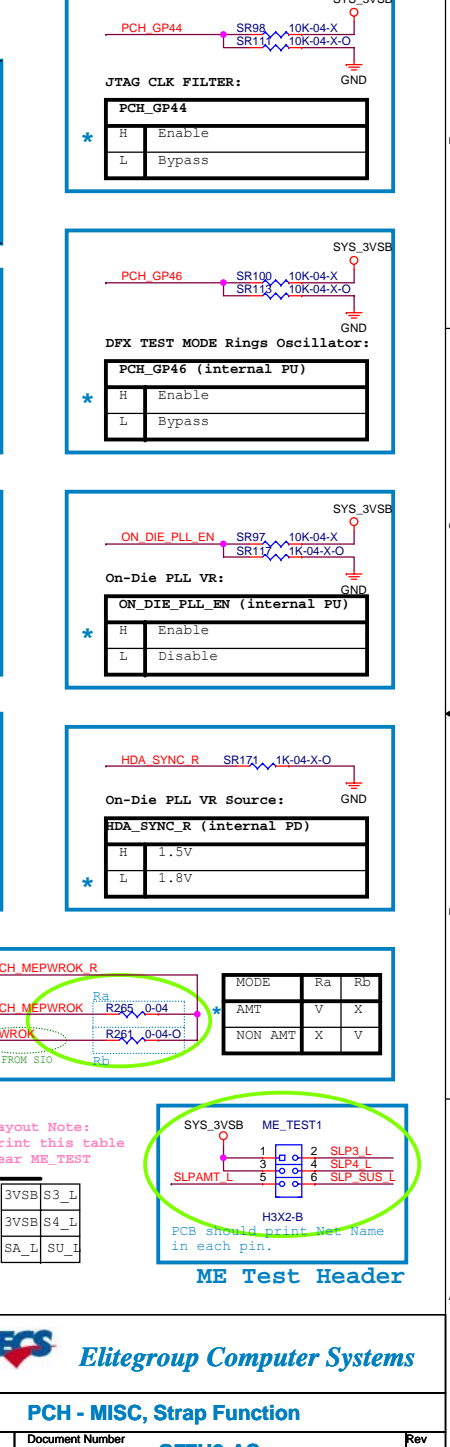
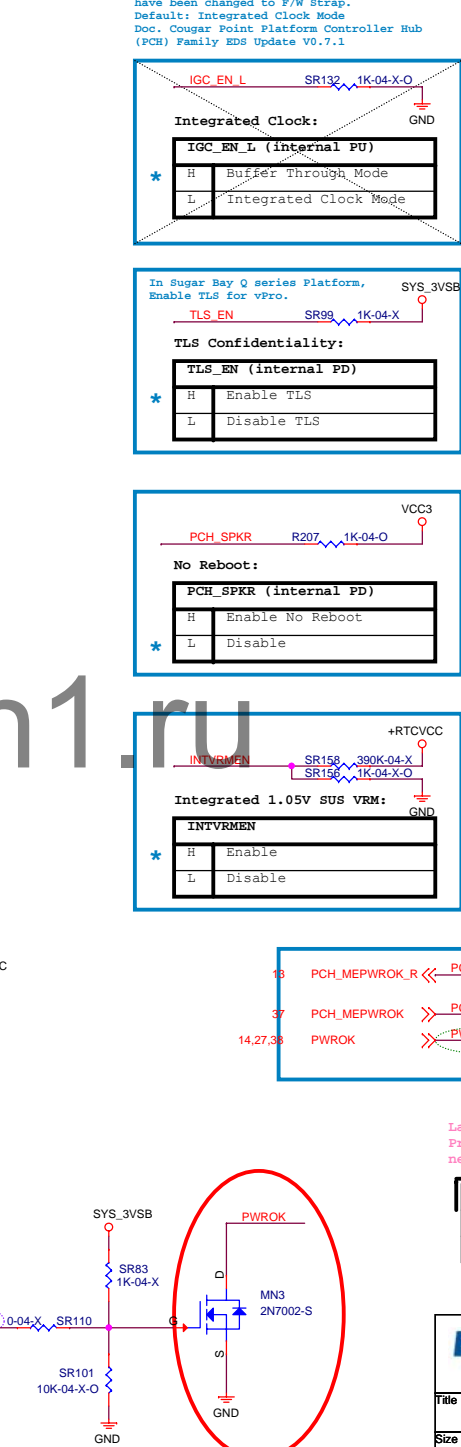
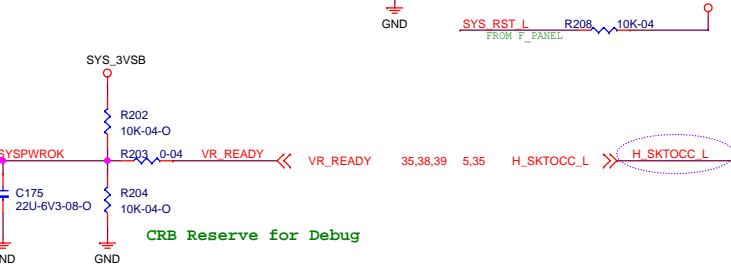
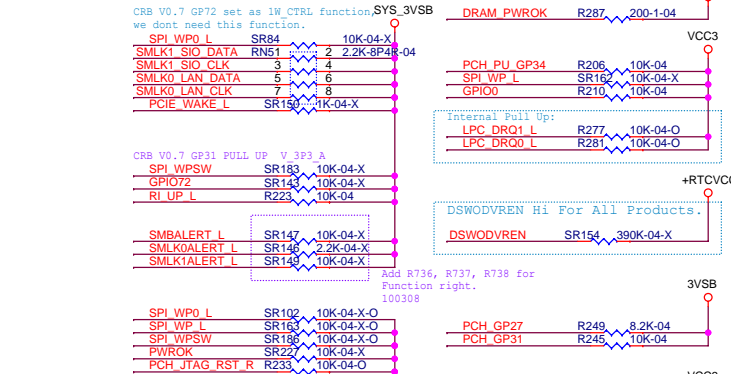
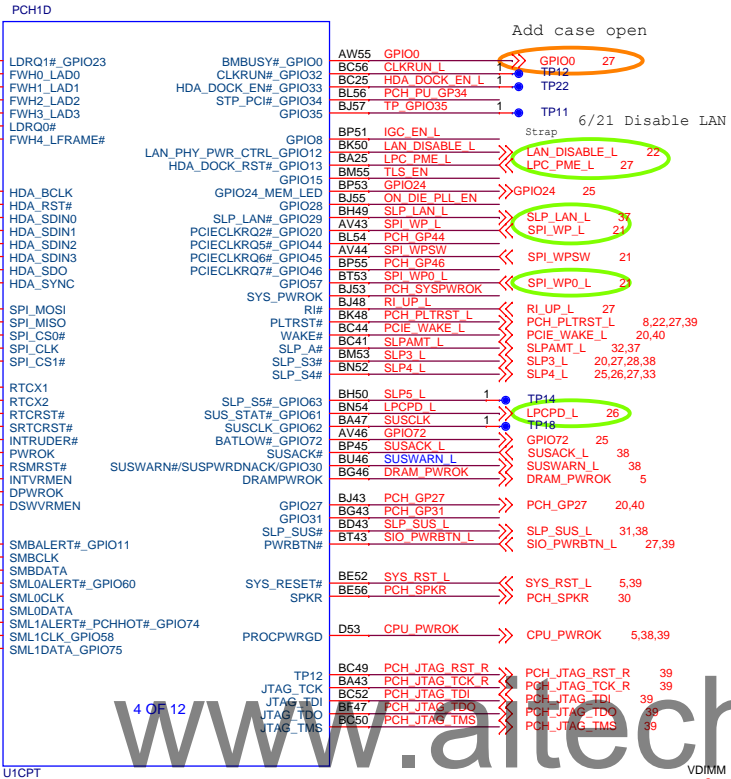
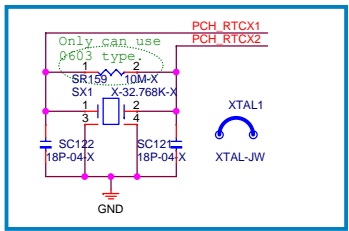
If you choose DIMM_VREF_DQ_B to be source, you must stuff Mb & Nb to be DIMM_VREF_DQ's source.



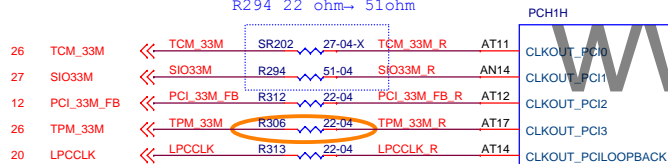




RSMRST# L SR164 0-04-X DPWROK
For platform not supporting
deep sleep connect directly
to RSMRST#.



12/13 Fix SI
SR202 22 ohm→ 27ohm
R294 22 ohm→ 51ohm



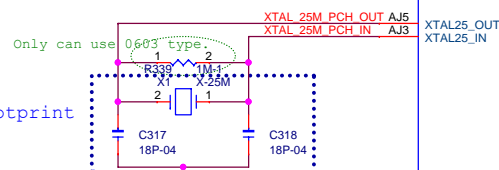
12/13 Fix SI
SR203 22 ohm→ 62ohm



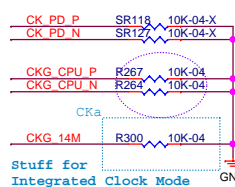
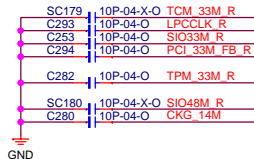
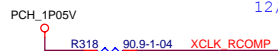
External pull-down input termination is required in Integrated Clock Generation mode and when no external clock chip is present



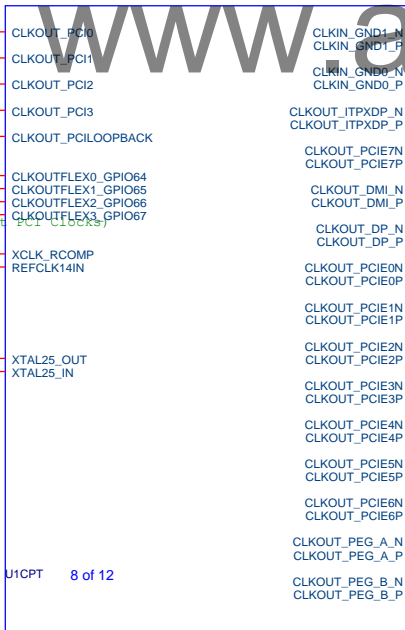
Layout Note:
PCI Clock Max 15000MILS



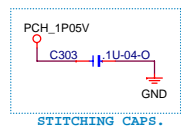
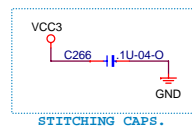
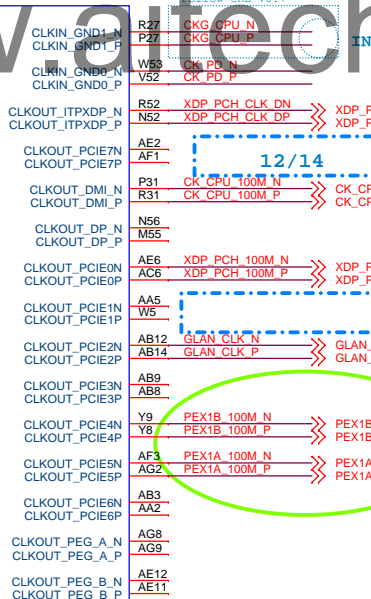
10/20 Modify footprint
07-165-250024



PCH1H



Follow CBB V0.7



Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

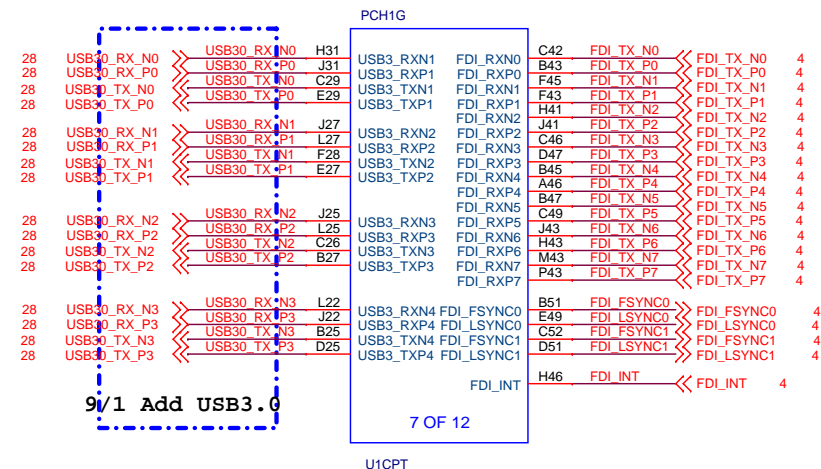
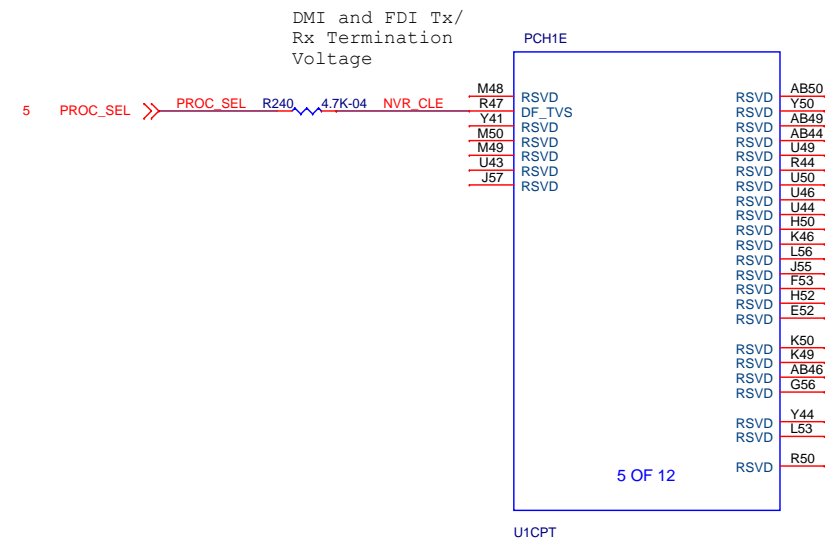
Elitegroup Computer Systems

PCH - CLK IO, SLG8XP421

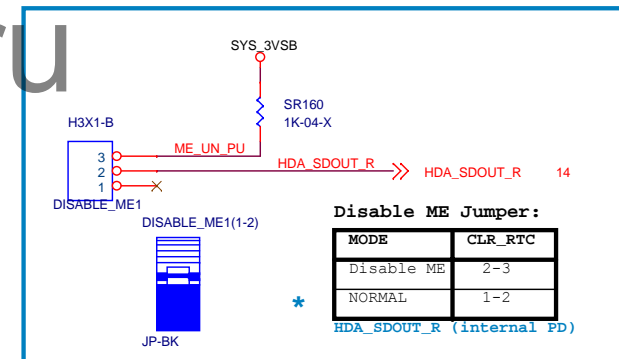
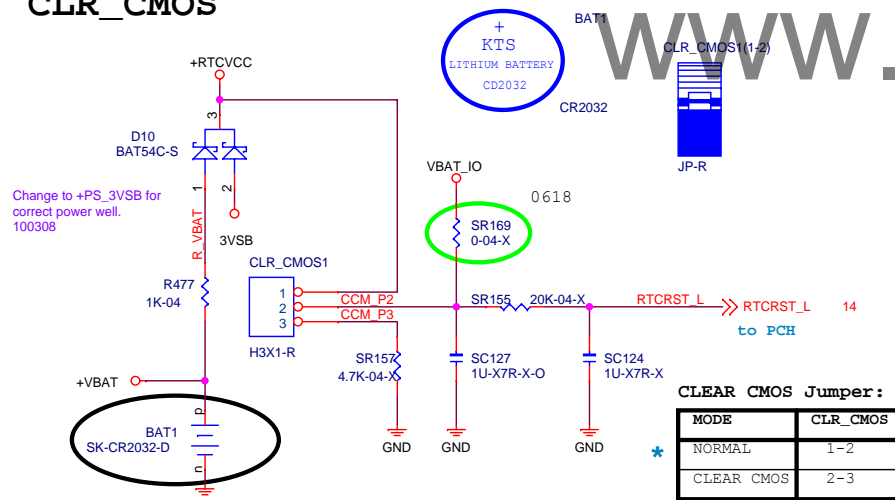
Size Custom Document Number **Q77H2-AS** Rev 1.0

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This pin should be pulled up to 1.8 V or 3.3 V.



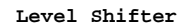
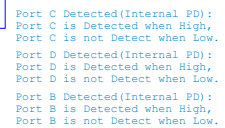
CLR_CMOS



Disable ME Header,
Always Stuff for ME or
non-ME Platform.

Elitegroup Computer Systems

Title		
PCH - NVRAM/FDI, CLR_CMOS		
Size	Document Number	Rev
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Date:	Thursday, February 08, 2012	Sheet 16 of 45





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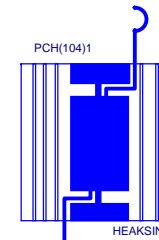
Title


Size	Document Number
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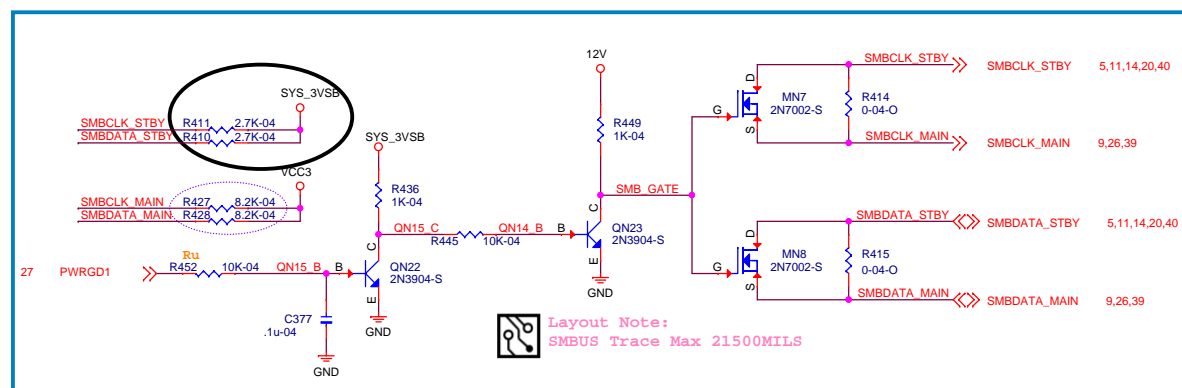
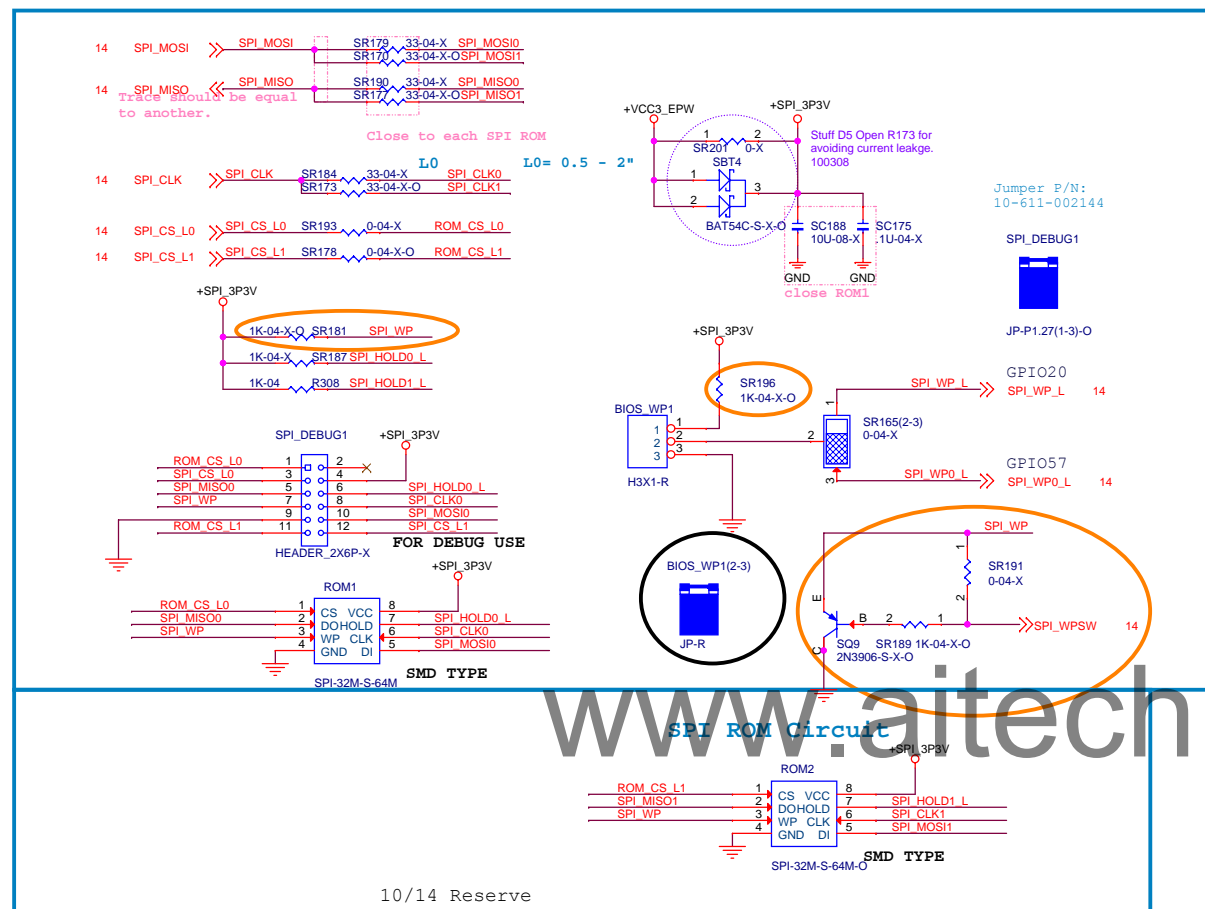
Q77H2-AS

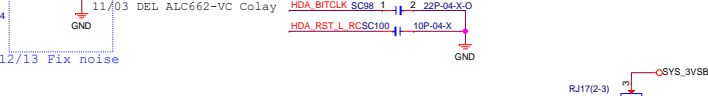
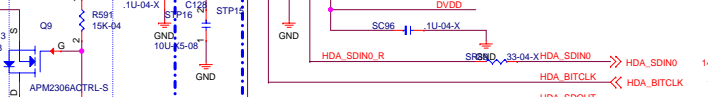
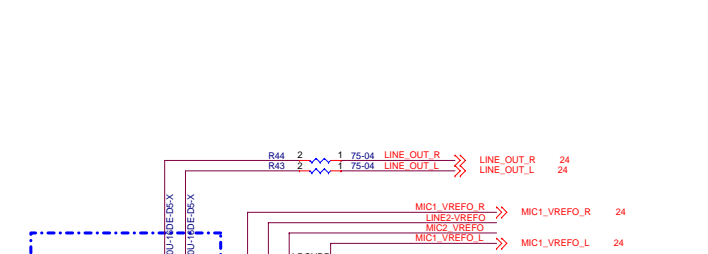
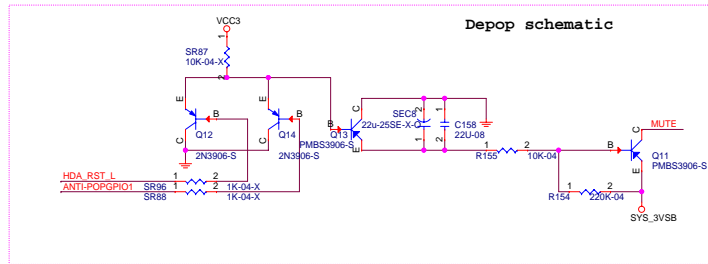
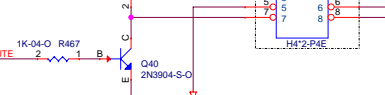
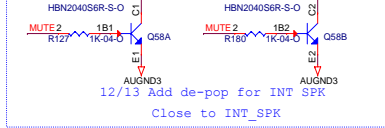
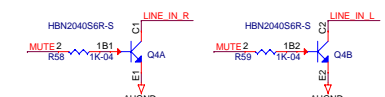
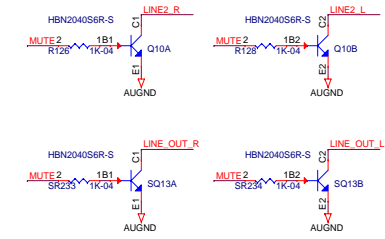
Rev
1.0

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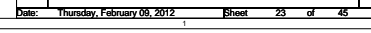
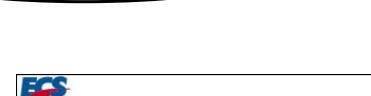
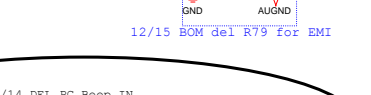
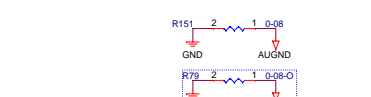
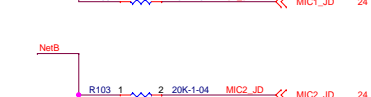
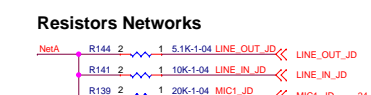
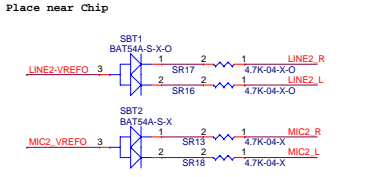
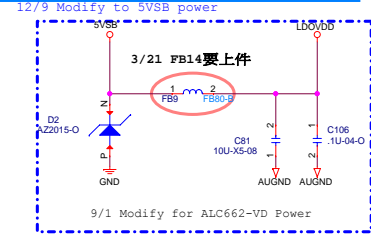


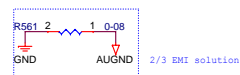
 Elitegroup Computer Systems			
Title: PCH - GND			
Size Custom	Document Number Q77H2-AS	Rev 1.0	
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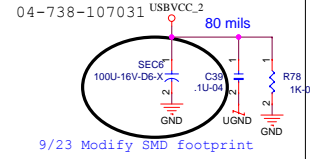
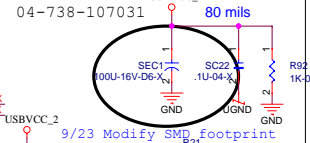
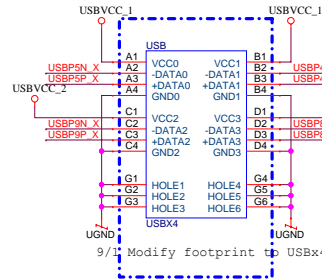
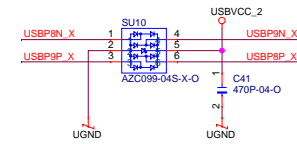
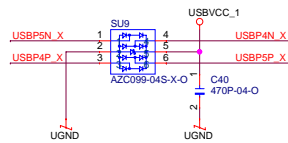
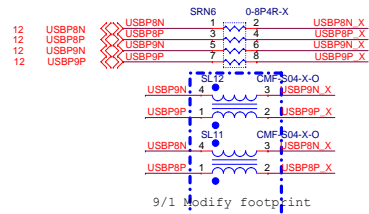
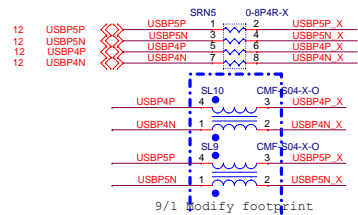
11/03 DEL ALC662-VC POWER



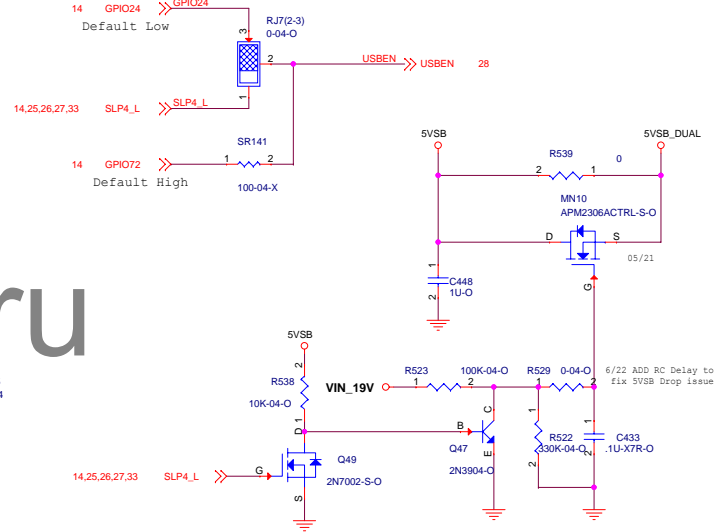
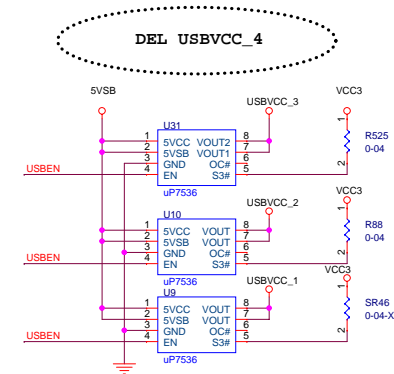


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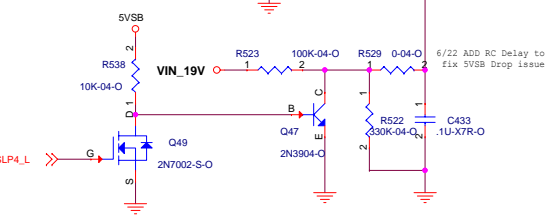
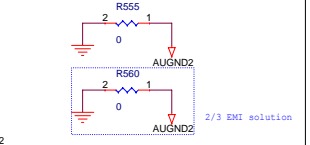
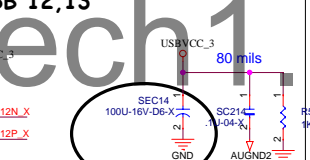
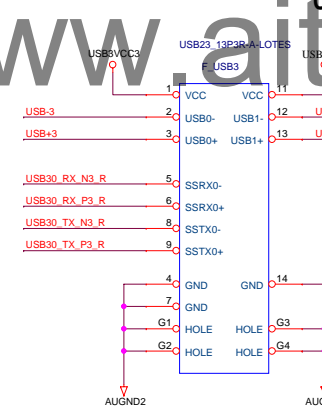
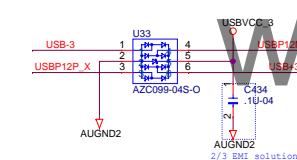
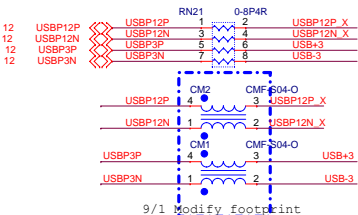
USB 4,5,8,9



0507 ADD EUP 1.5A Continuous Load Current

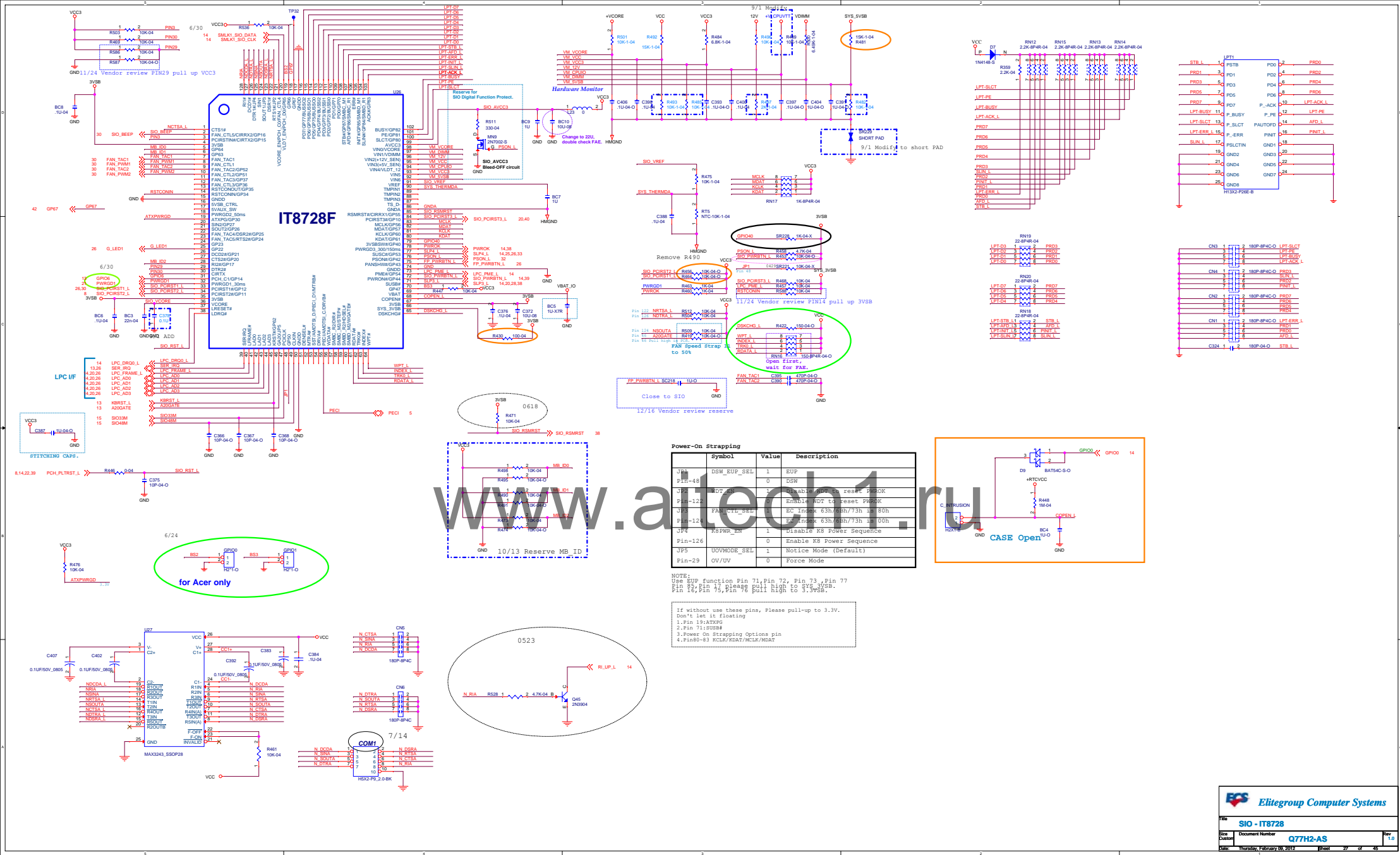


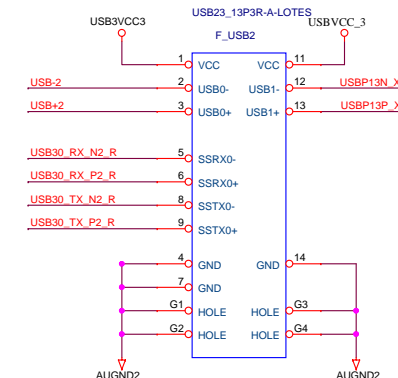
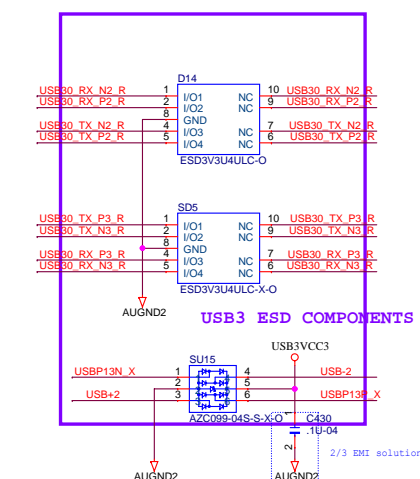
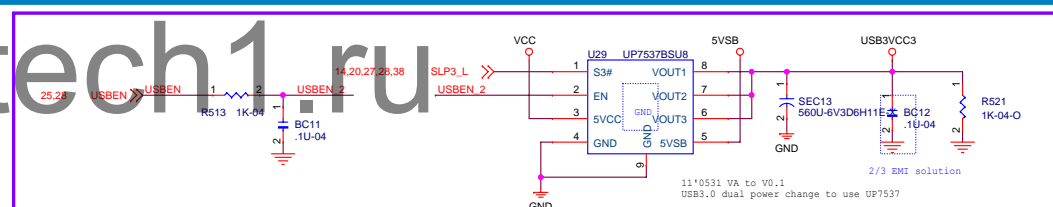
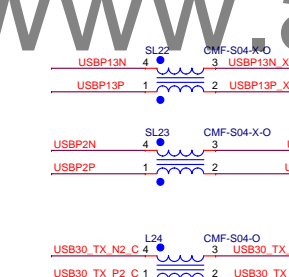
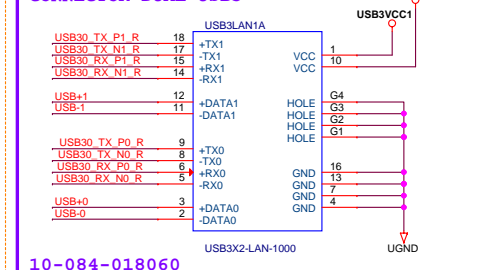
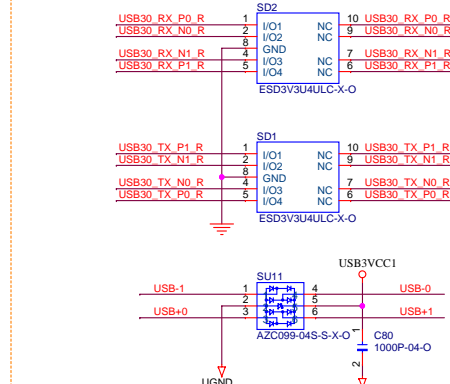
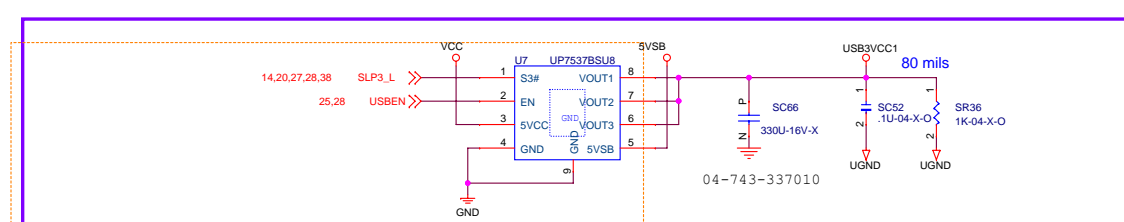
USB 12,13

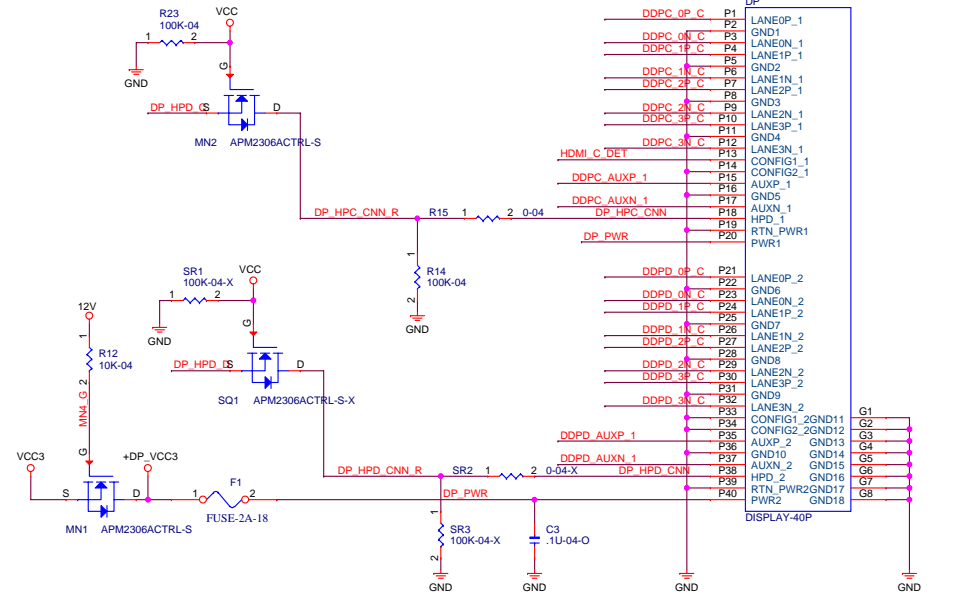
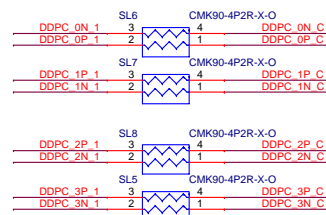
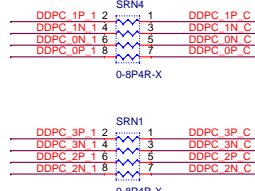
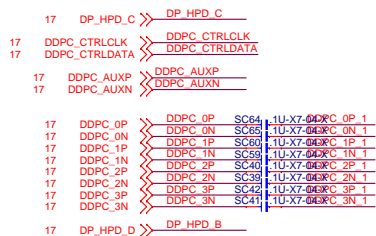


Elitegroup Computer Systems		
USB Port		
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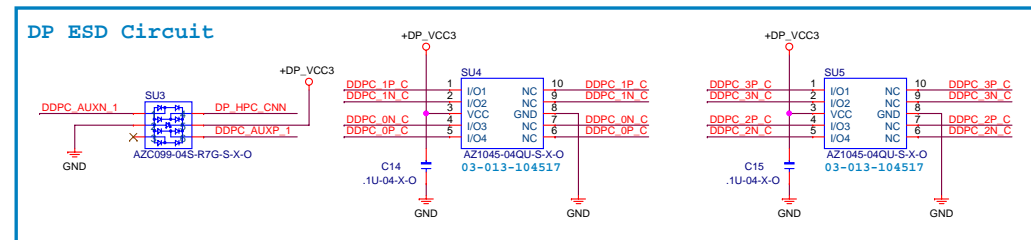
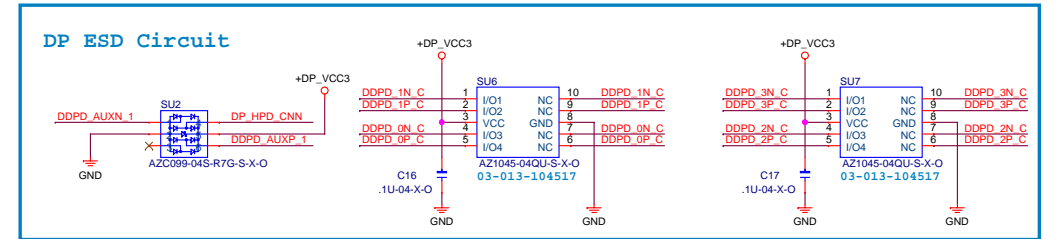
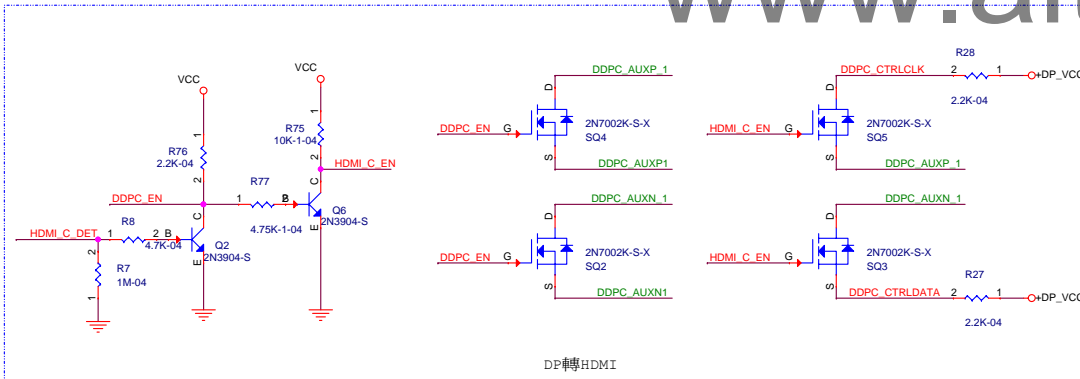
Front Panel



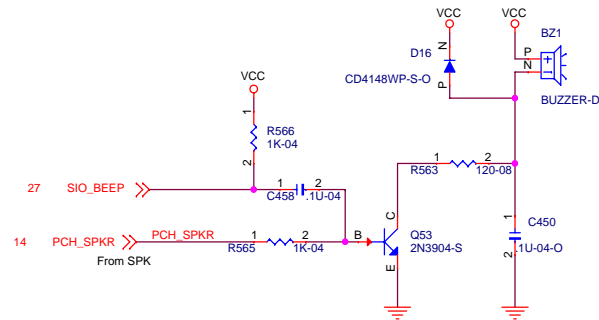




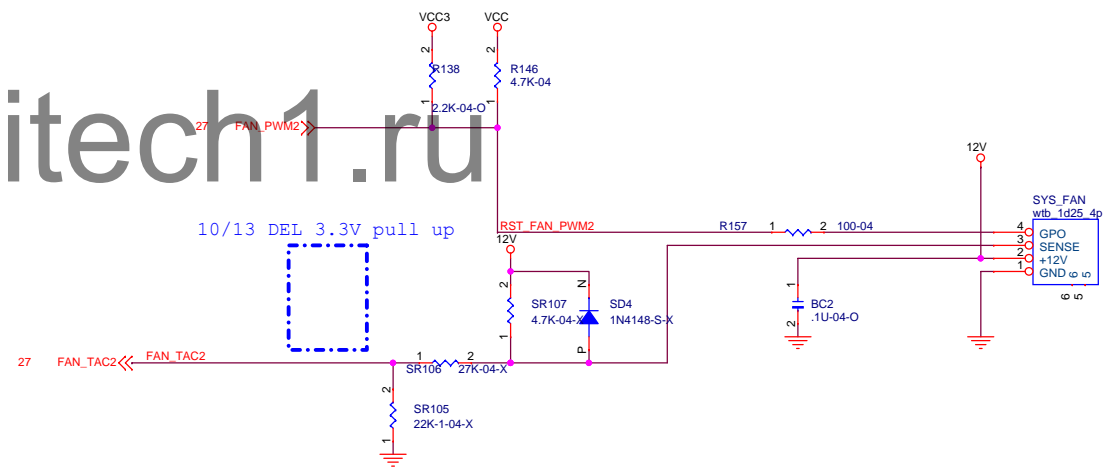
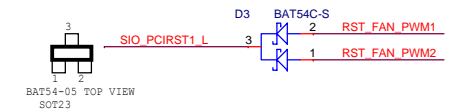
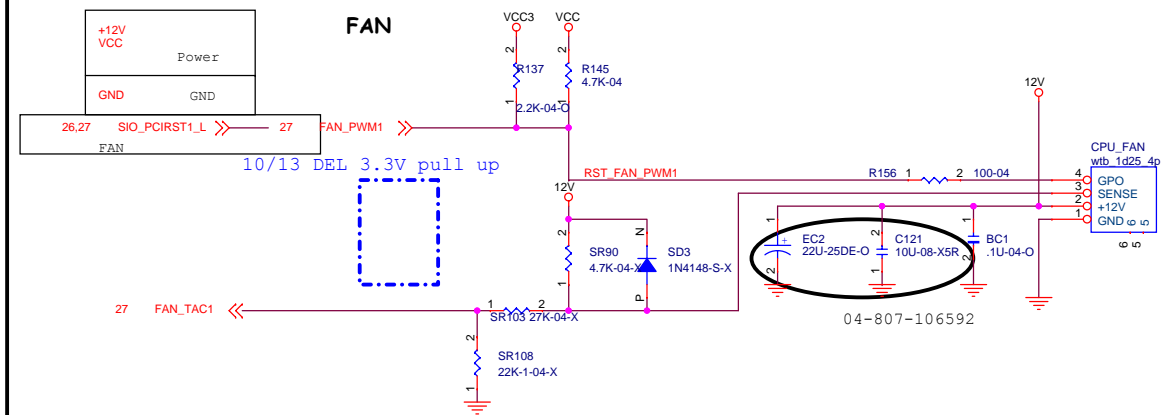
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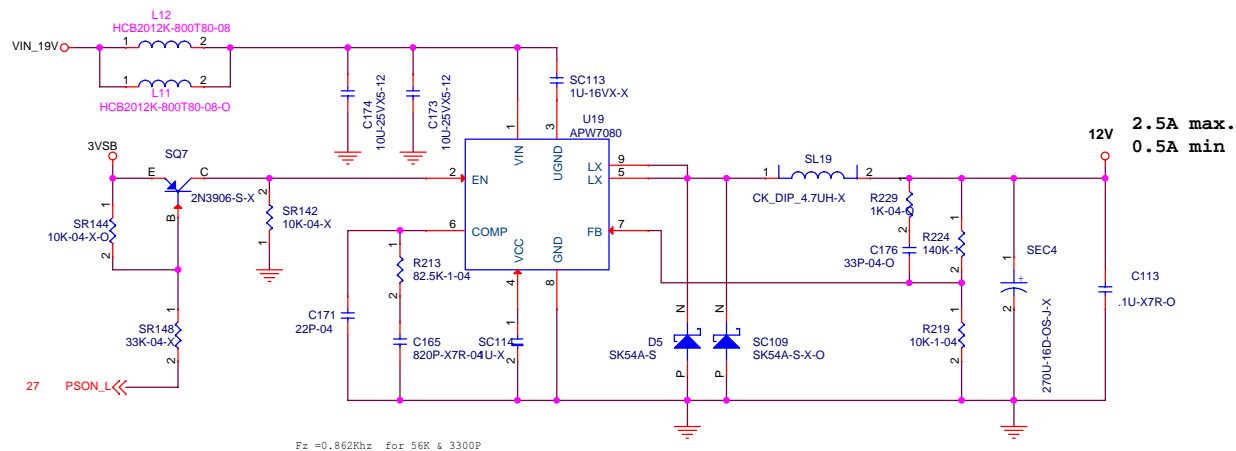
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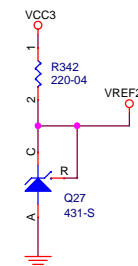
FAN



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VREF25

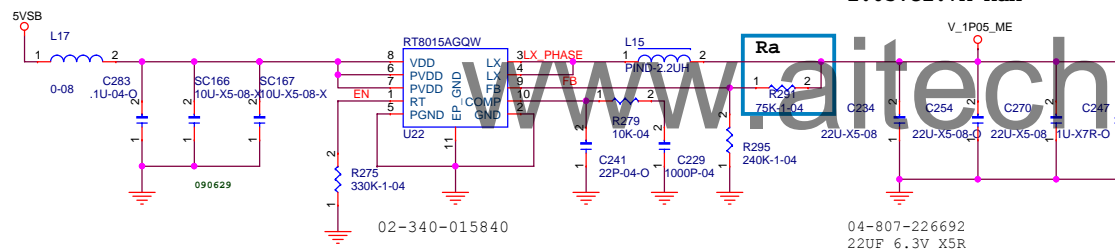


12/9 B75上件

V_1P05_ME

08-463-225092
2.2uH DCR 60mOhm

1.05V@1.7A Max

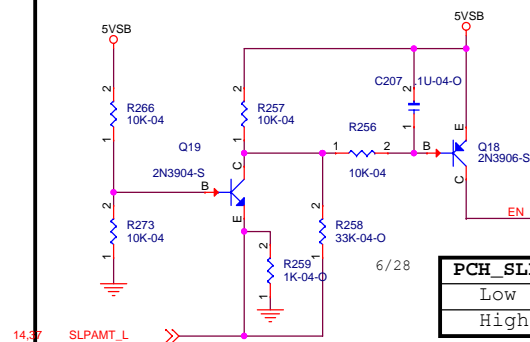


EMPTY EVERYTHING ELSE ON PAGE FOR NON AMT
STUFF KFB2 FOR NON AMT SYSTEM

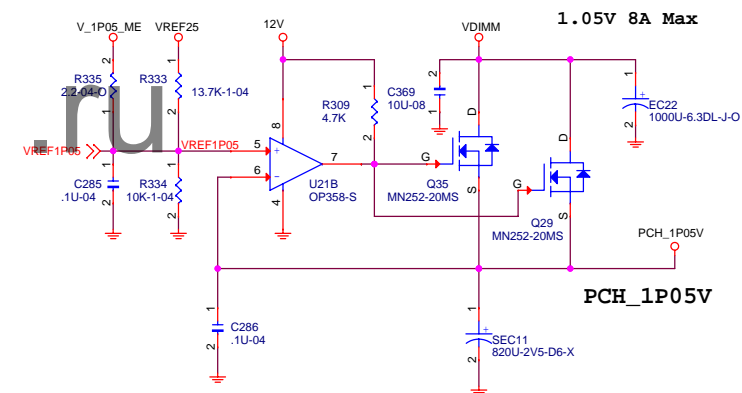


For Non-AMT

Ra	V_1P05_ME
75	1.05V
90	1.1V

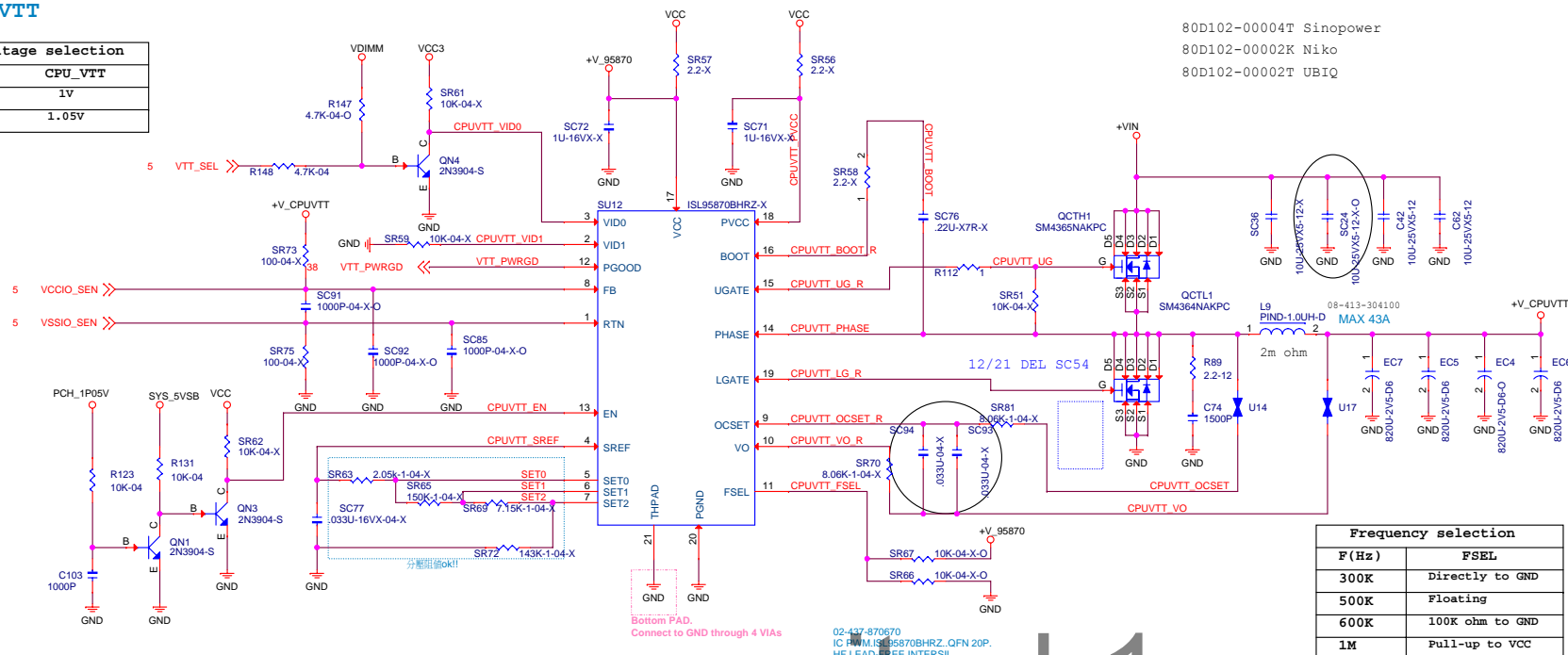


PCH_SLP_M_L	EN	V_1P05_ME
Low	5VSB	Disable
High	0 V	Enable



V_CPUVTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V

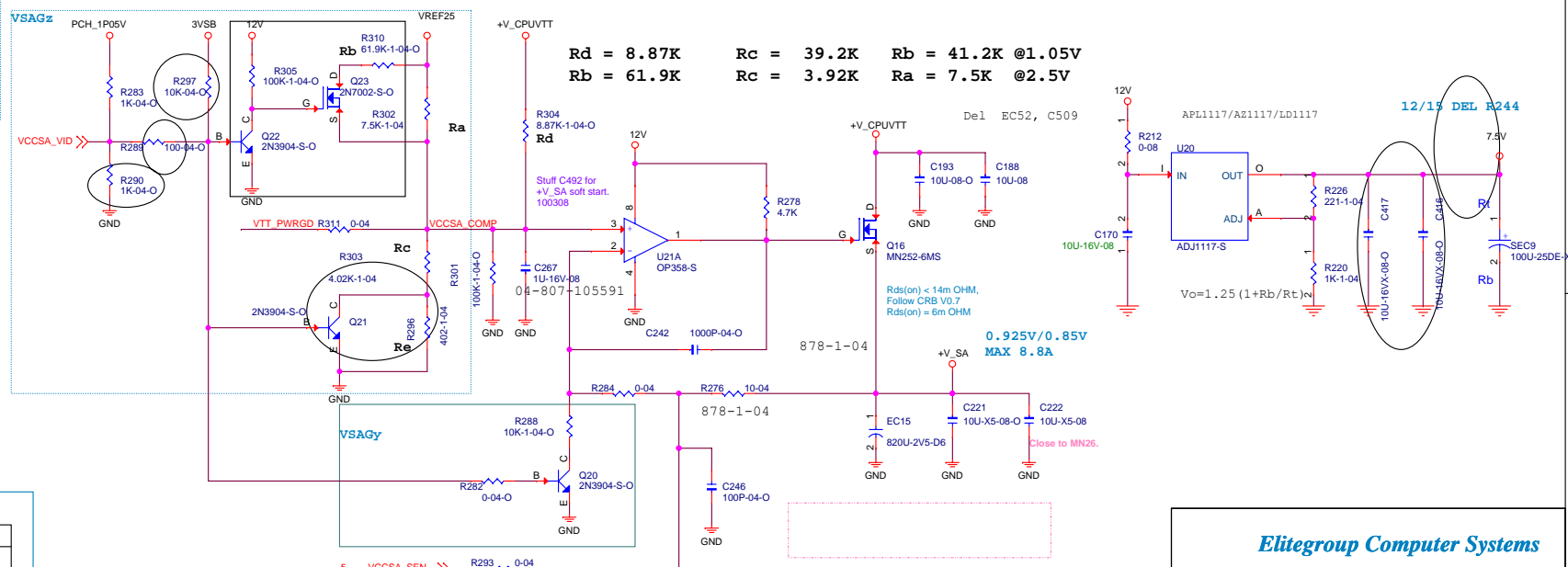


Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

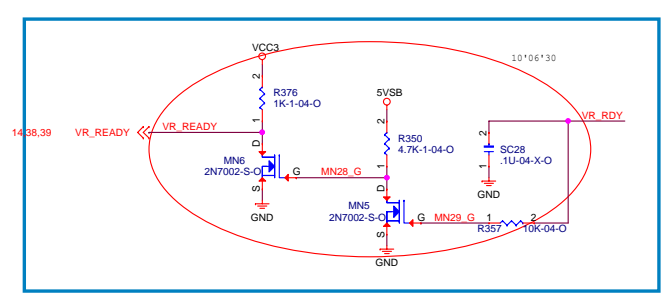
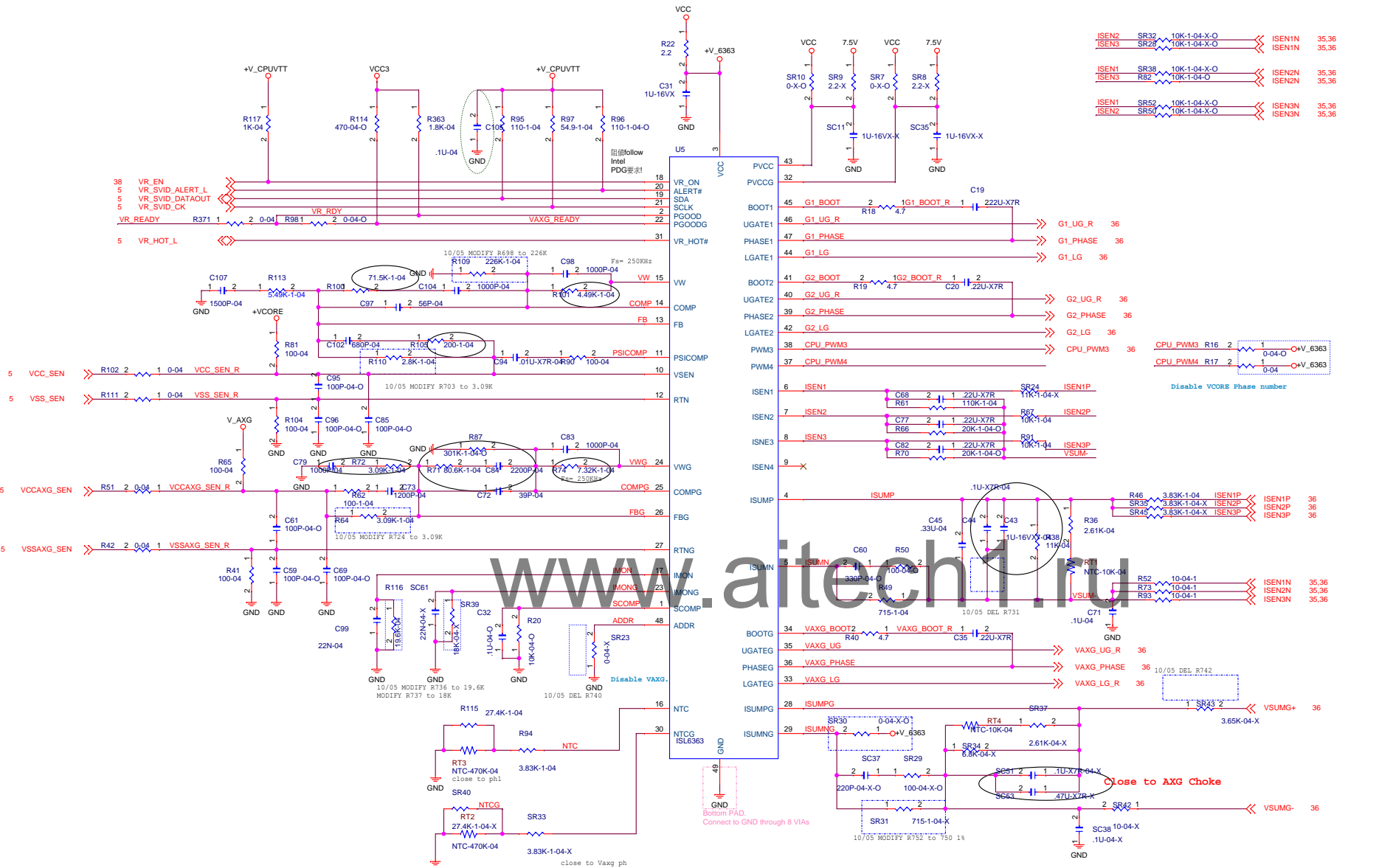


Stuff VSAGy

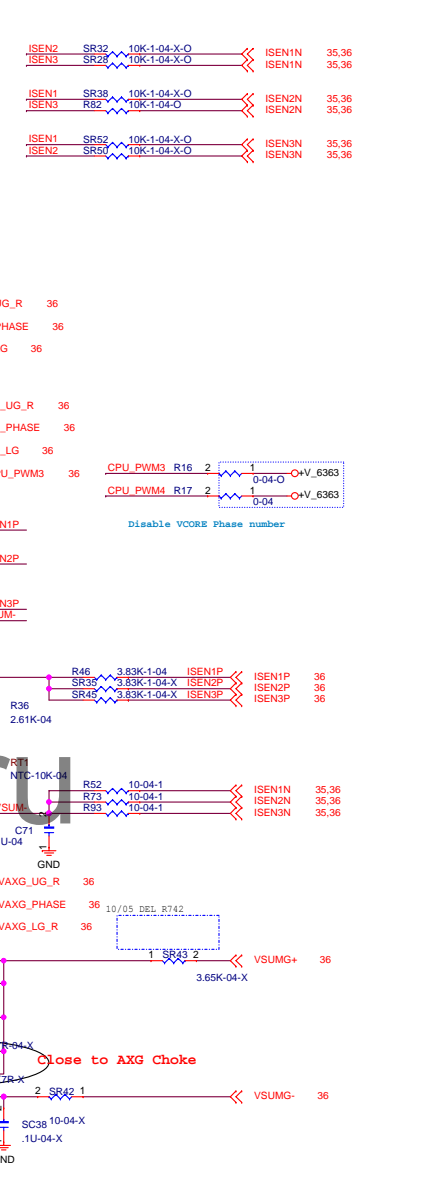
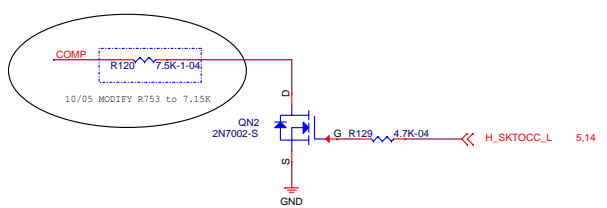
VCCSA voltage selection	
VID	+V_SA
0	0.85V
1	0.925V

Elitegroup Computer Systems

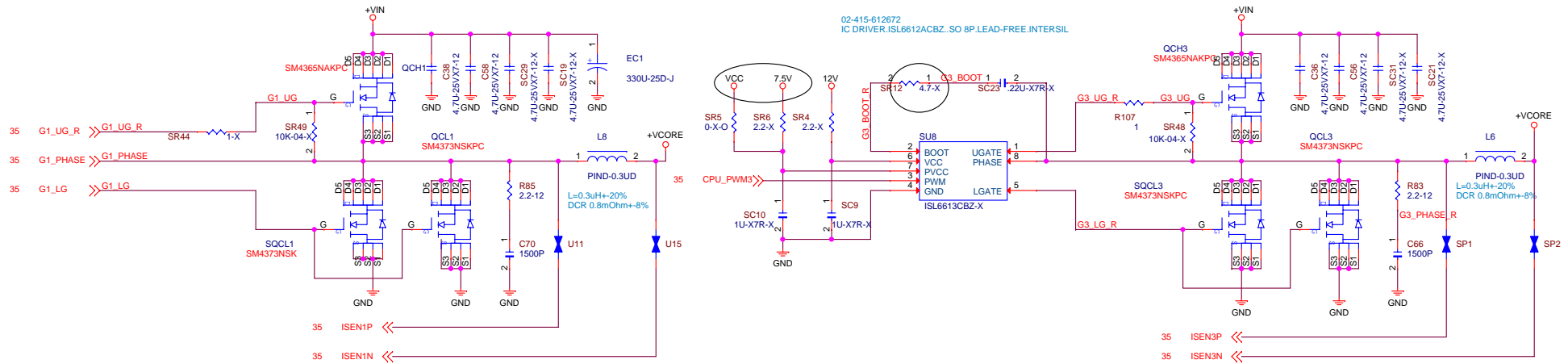
Title		DC/DC V_CPUVTT
Size	Document Number	Q77H2-AS
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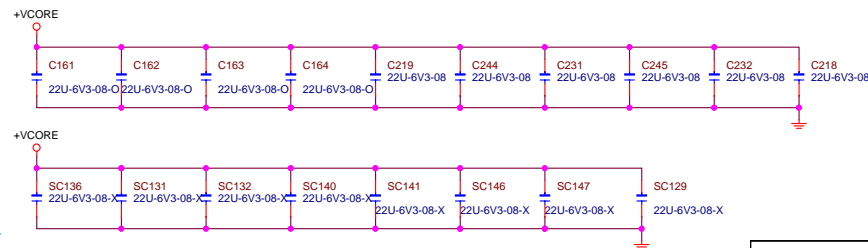
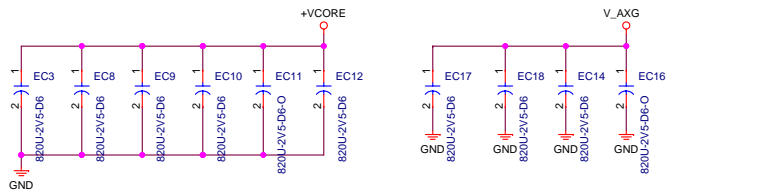
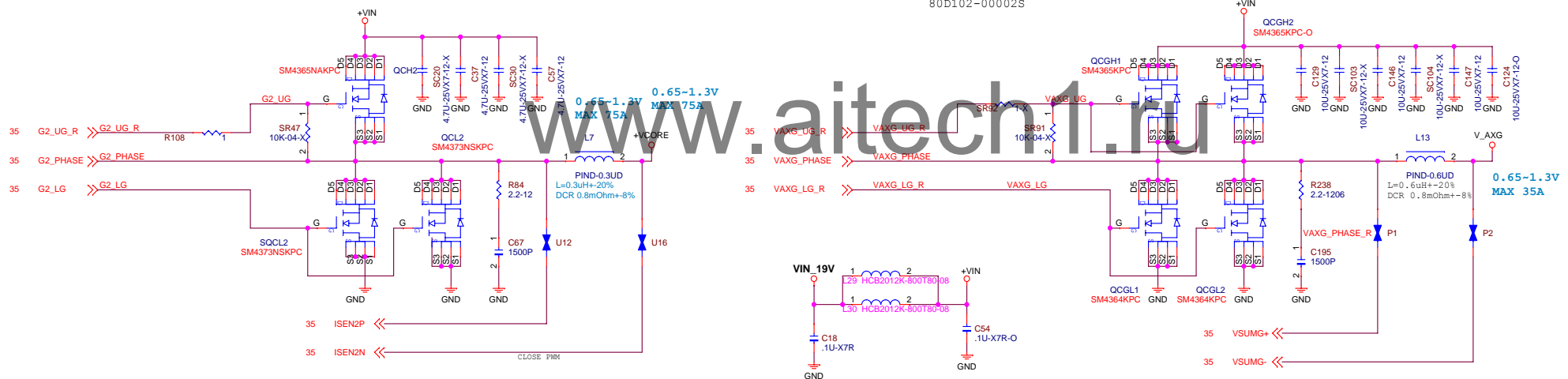
For VR_READY Power On Sequence



80D102-00004A Sinopower
80D102-00004B Niko

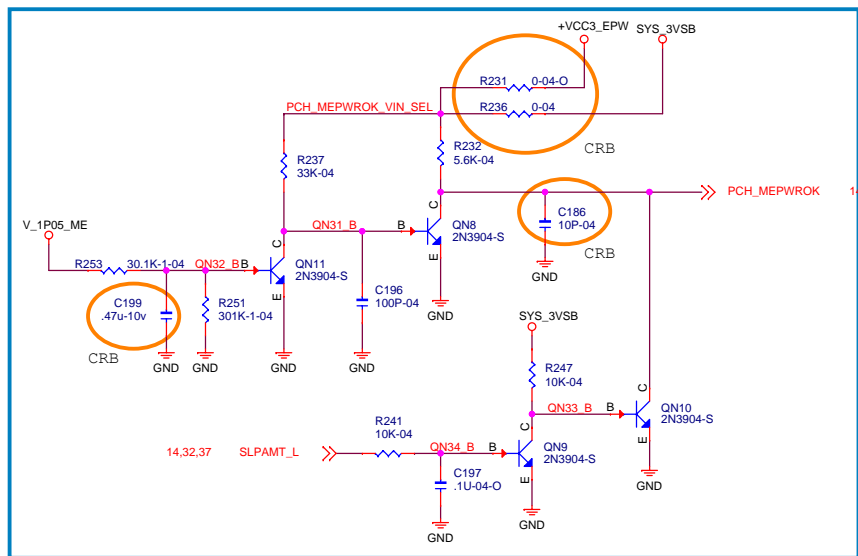


80D102-00002R
80D102-00002I
80D102-00002S

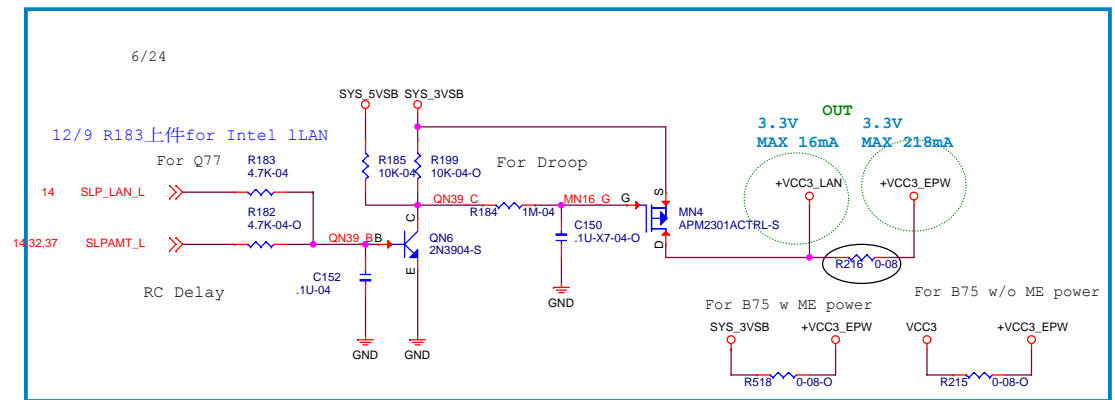


Elitegroup Computer Systems

Title			DC/DC V CORE/V AXG2
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PCH_MEPWROK Circuit



VCC3_EPW control

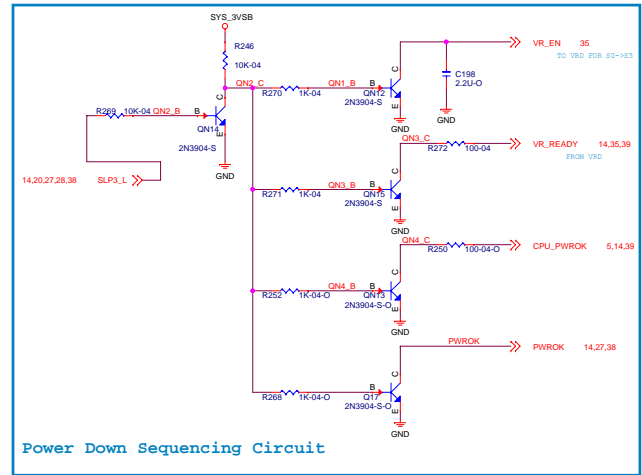
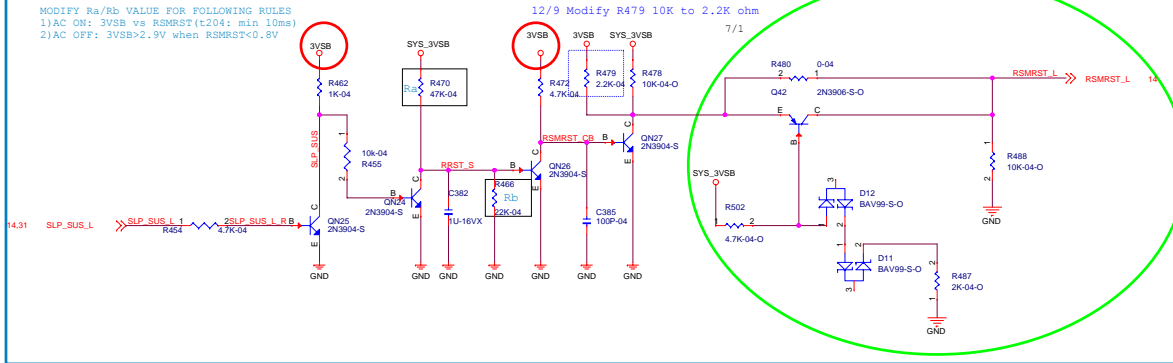
**VCC3 Net to +VCC3_EPW FOR
NON-INTEL LAN (NO WOL) OR M0 ONLY**

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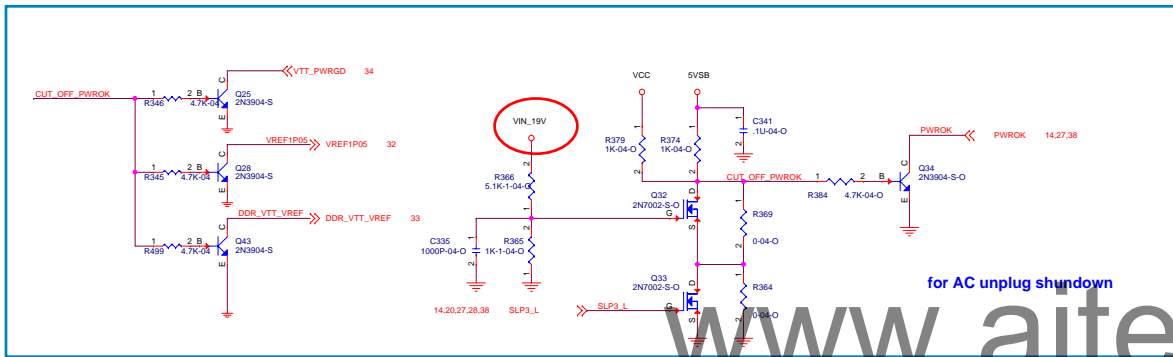
		Elitegroup Computer Systems	
Title		DC/DC 3VDUAL	
Size	Document Number	Q77H2-AS	Rev
Custom			1.0
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RSMRST Circuit

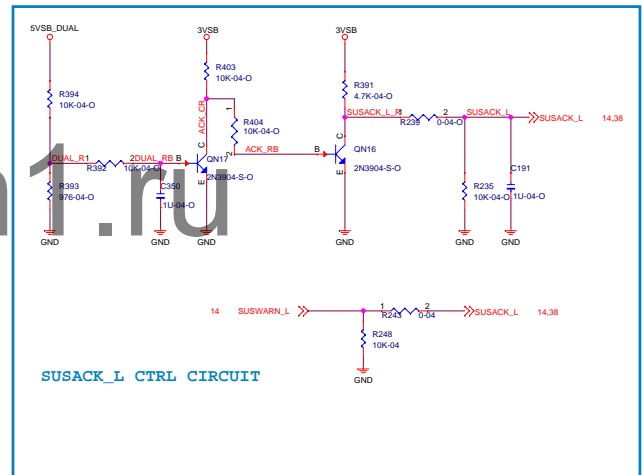
MODIFY Ra/Rb VALUE FOR FOLLOWING RULES
1)AC ON: 3VSB vs RSMRST (t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V



Power Down Sequencing Circuit

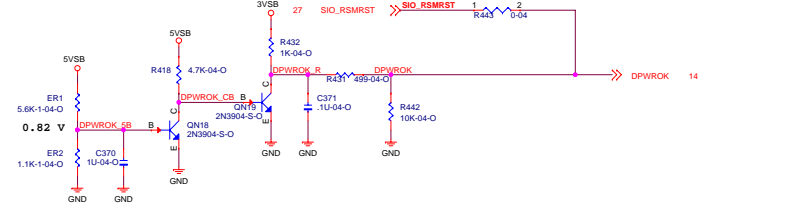


for AC unplug shutdown

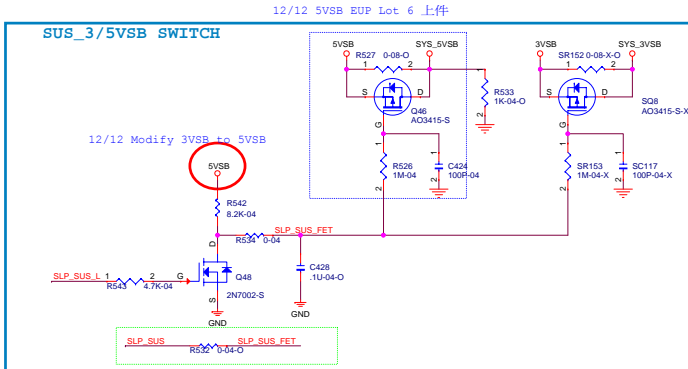


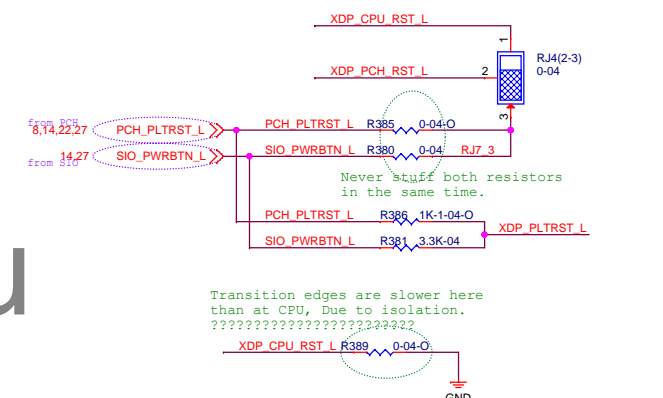
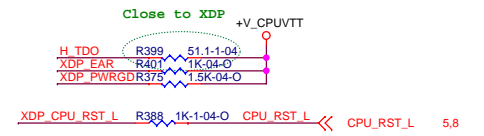
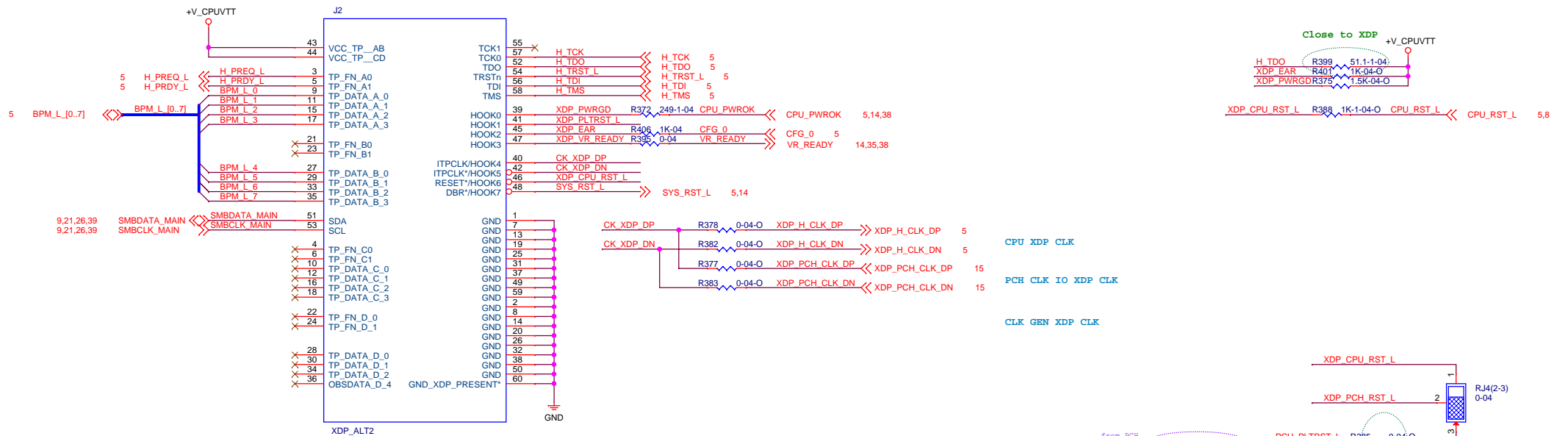
SUSACK_L CTRL CIRCUIT

DPWROK Circuit

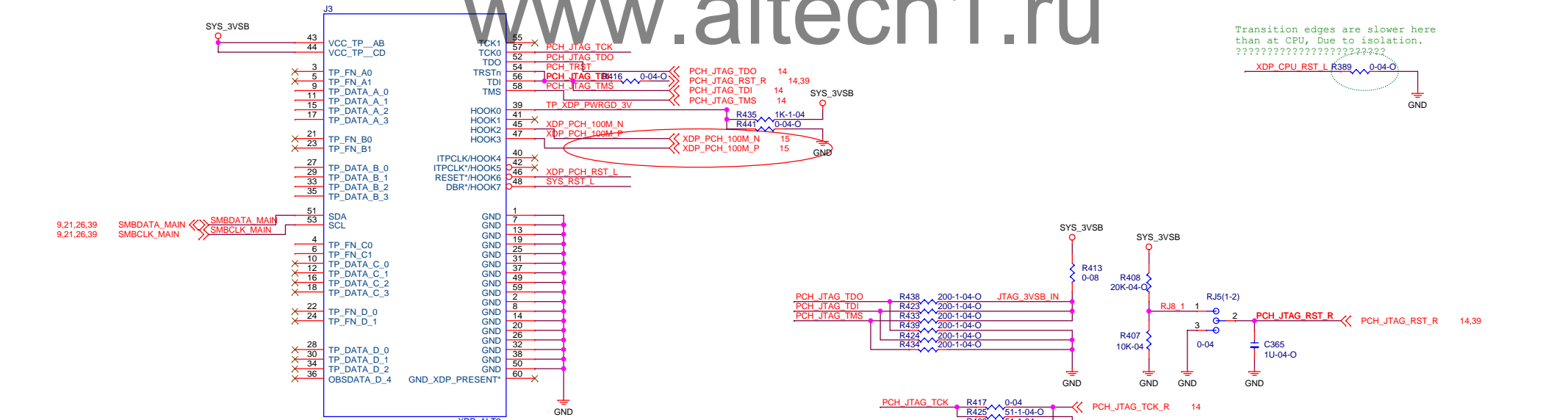


SUS_3/5VSB SWITCH



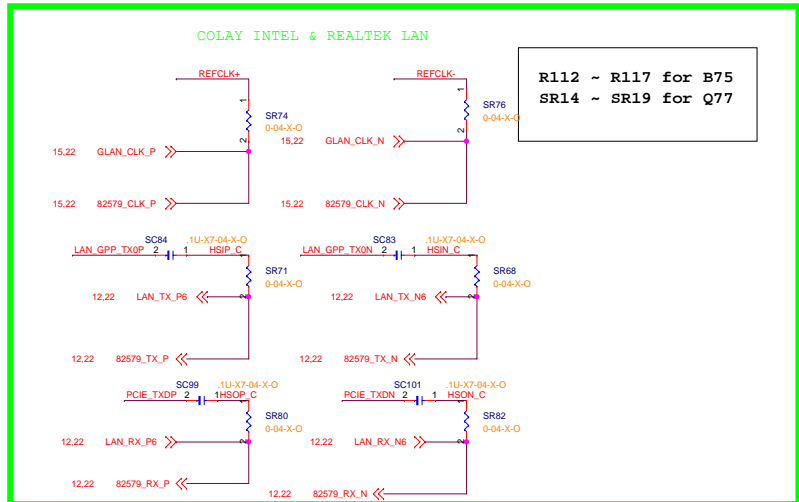
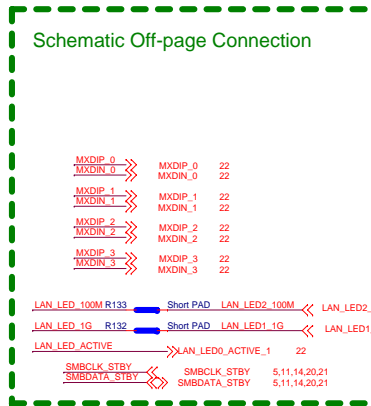
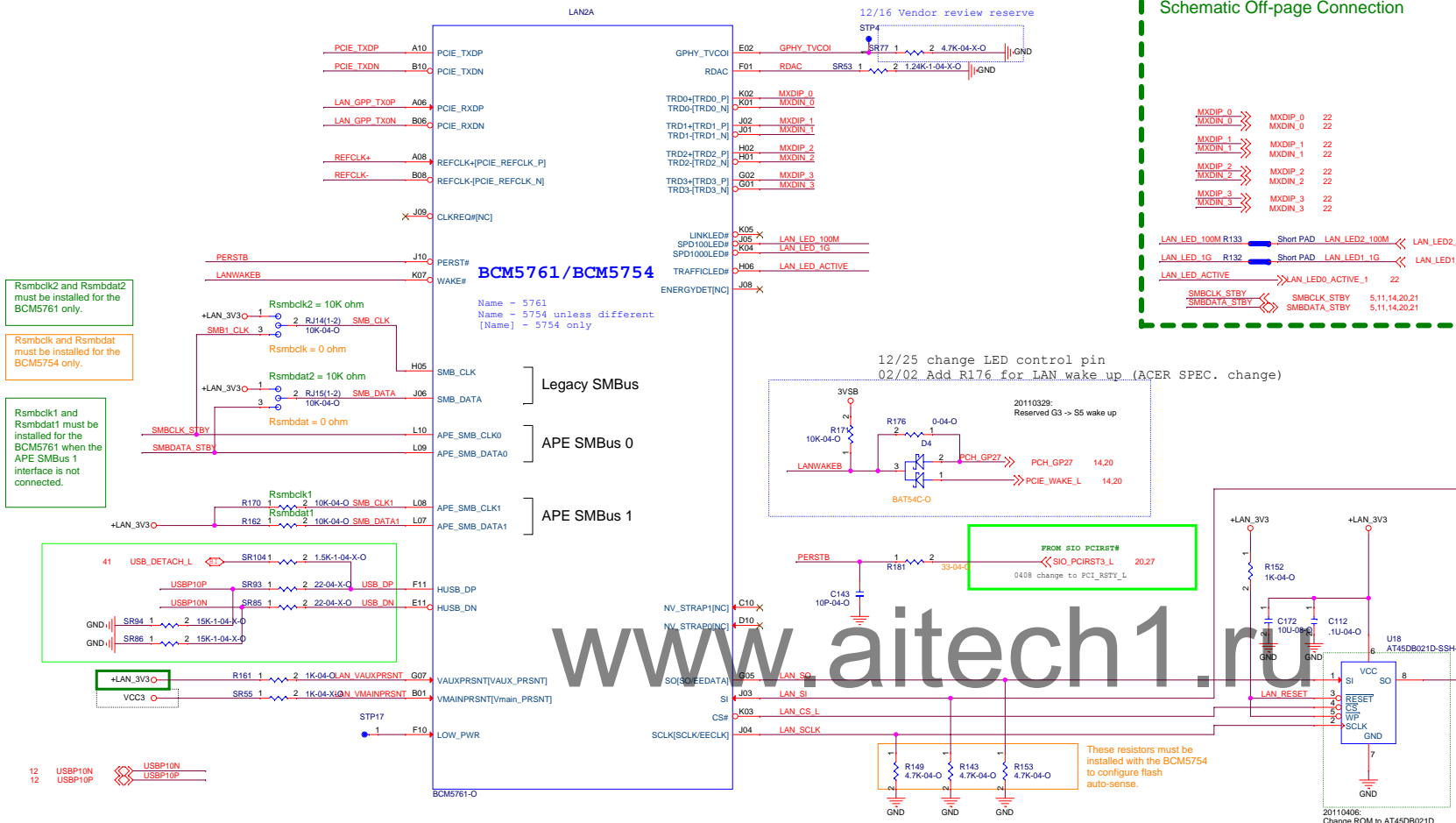


Transition edges are slower here than at CPU, Due to isolation.
 ??????????????????????



DESIGN NOTE:
PCH JTAG

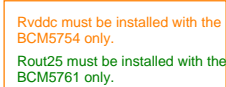
DESIGN NOTE:
DEFENSIVE DESIGN



*



```
Name - 5761
Name - 5754 unless different
[Name] - 5754 only
```



Qnp25 and Cnp25 must be installed with the BCM5754 only

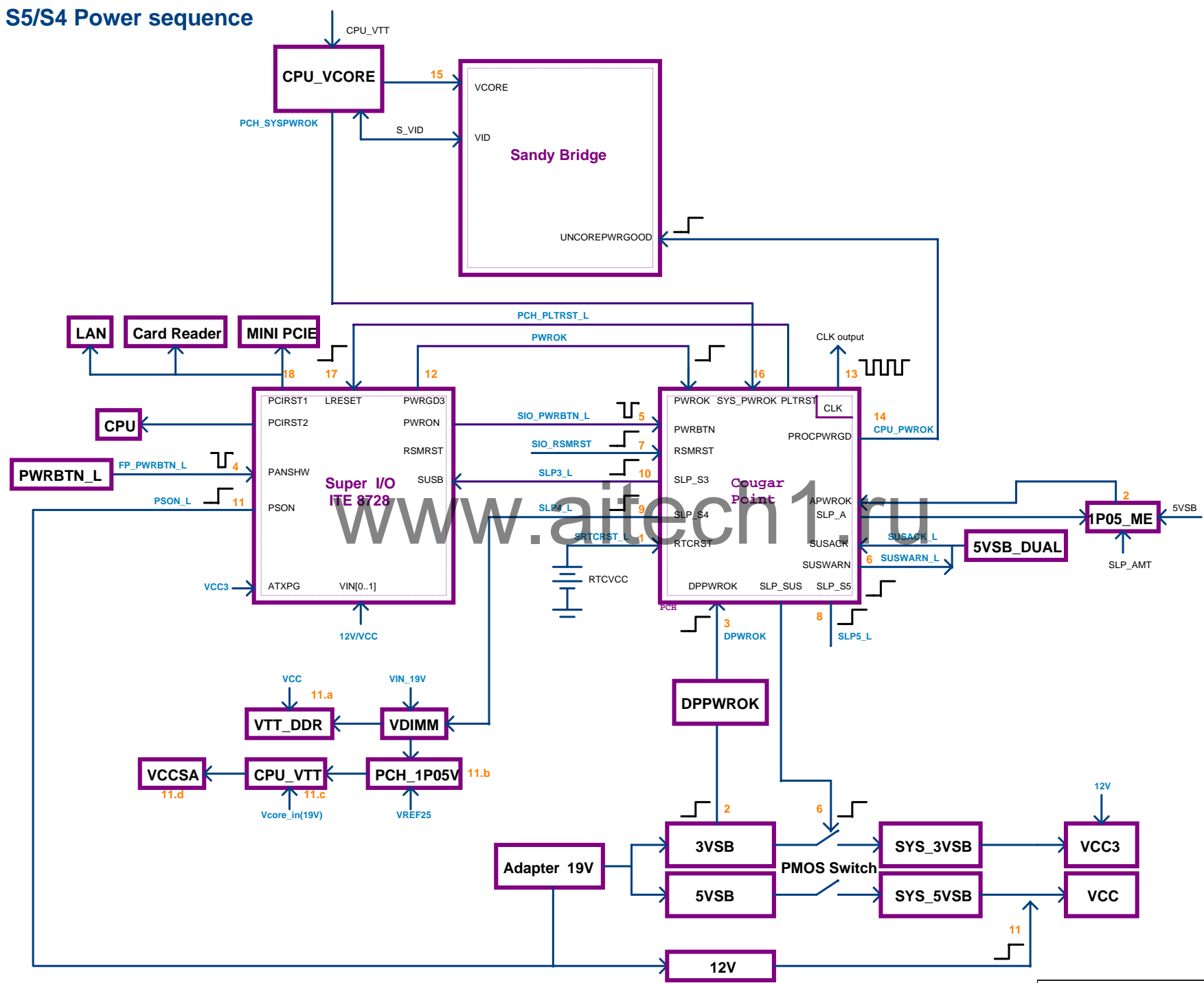
Cdebug12 and Cdebug25 are place holders only for debug purpose.

Rvddp must be installed with the BCM5754 only.

Rpwr_down_pd must be installed with the BCM5761 only.

The PWR_DWN[VDDP] ball must not be driven to 3.3V. Refer to the BCM5761 data sheet for logic thresholds and maximum ratings.

Deep Sleep S5/S4 Power sequence



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

